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CID PROCESSOR CHIP DEVELOPMENT

General Electric Company
Corporate Research and Development
Schenectady, New York 12301

November 1977

FINAL REPORT FOR PERIOD 15 MARCH 1976 - 1 MAY 1977

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coding techniques can then be used to allocate the available bandwidth to the significant spatial information. A number of transforms such as the Hadamard, Fourier, Haar, Cosine and Slant could be used. Until recently, however, the real time realizations of these transformations were questionable. The use of large numbers of logic, memory, and linear devices would be required to process the video signal in a conventional manner. Charge-injection device technology can be used to combine such widely diverse functions as imaging, memory, and signal processing into a single device to achieve low system cost, size, weight, and power consumption.

The process of computing the Hadamard transform requires linear combinations, sums and differences, of the picture information. This process can be easily mechanized on the focal plane of a CID image sensor by sensing combinations of the signal charge from a number of image sensing sites (pixels) rather than the individual pixel magnitudes.

This two-part program consisted of a design study, in which array parameters and array/systems interface were specified, and of a fabrication and evaluation phase. The resulting video sensor is a charge injection device (CID) solid state imager which can be operated in two modes. In one mode the output is a conventional video signal. In the second mode the same chip is operated in such a manner that the signal output is the Hadamard transform of the optical image. This result is made possible because of the non-destructive readout (NDRO) capability of the CID, along with its ability to perform repeated algebraic summations of the photon-generated charge packets without signal mixing.

The imager consists of a 128×128 array of 30 micron square sensing sites. The significant performance factors are a dynamic range of 500-to-1, dark current density of 1 nA/cm^2 , high quantum efficiency (45% @ 0.66μ), and a very narrow point spread function. The imager is capable of producing four 1×4 Hadamard transforms in parallel, which are then summed to produce a 4×4 area transform of each sub-picture.

The feasibility of real-time transform coding of an optical image directly on a CID imager has been conclusively demonstrated.

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FOREWORD

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This report was prepared by the scientific and engineering staff of the General Electric Company for the Air Force Wright Aeronautical Laboratories under Air Force Contract No. F33615-76-C-1188. The work was performed at General Electric Corporate Research and Development Laboratories, Schenectady, New York and Aerospace Electronic Systems Products Department, Utica, New York.

The work, performed between 15 March '76 and 1 May '77, was directed for the Air Force by Dr. R.A. Belt, Air Force Avionics Laboratory.

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1.0 INTRODUCTION

This final report describes the General Electric Company's efforts on a twelve-month program for the development of a CID imager capable of performing signal processing functions in addition to the imaging function. Specifically, this CID imager produces directly a Hadamard transform of an incident optical image and, in addition, is capable of producing a normal video signal, when operated in a second mode.

This two-part program consisted of a design study, in which array parameters and array/systems interface were specified, and of a fabrication and evaluation phase. The design study phase was performed, in large part, by the Aerospace Electronic Systems Product Department, Utica, New York; while the remainder of the work was carried out at Corporate Research and Development, Schenectady, New York.

The design study indicated that a simple, high-density array would be effective both as a normal imaging device and for Hadamard transform readout. It was possible to increase the number of array elements from 64×64 to 128×128 , with performance goals unchanged, within the resources of the original contract. The performance achieved with the larger array demonstrates that this was a proper decision. This program has demonstrated that focal-plane signal processing can be effective, and high performance achieved, in high-density, high quantum efficiency solid-state CID imagers.

2.0 STUDY RESULTS

2.1 PURPOSE AND OBJECTIVE OF DESIGN STUDY

The overall objective of the design phase was to specify the CID focal plane processor chip design parameters based upon overall system performance and chip design complexity. To satisfy this objective, the study was conducted in two parts. The first part was directed at determining the interface requirements between the CID chip and a generic system based on optimum system performance. This effort included a comparison of one-, two-, and three-dimensional transform encoding, the effect of block size on system performance and hardware complexity, and methods of performing the inverse.

The second part of the study consisted of an investigation of the various Hadamard transform encoding techniques and transform sizes with respect to CID chip complexity, manufacturability, and performance as a conventional imager.

2.2 PROBLEM DESCRIPTION

The CID focal plane processor is a low power, small size, bandwidth compression implementation approach suitable to mini-RPV applications. Prior to discussing the CID implementation a brief description of the jam resistant video data link problem is given.

The transmission of video data from an RPV to a distant observer requires a large bandwidth channel in order to protect the video information against jamming and interference. This protection can be achieved by Spread Spectrum techniques, whereby the information bandwidth is spread and transmitted over a wideband signalling structure and received in a correlation type receiver. In many applications, however, the available channel bandwidth is barely sufficient or is insufficient to transmit the video signal directly. In these cases the video information can be transmitted only after the redundancy present in the original image is greatly reduced. Transform encoding or block quantization has become a leading candidate for removing redundancy in images. The underlying principle of transform encoding is that the transform domain representation of an image has an energy distribution that is more compact and therefore easier to code than the spatial domain version. This technique has been shown, via software simulation, to be capable of providing adequate bandwidth compression but requires complex signal processing. Efforts directed at hardware implementation of these complex algorithms within the severe RPV size requirement have met with little success.

Shown in Figure 2-1 is a functional block diagram of a generic jam resistant video data link. The system consists of an encoder located in the RPV and a decoder located in a control aircraft or at a ground station. The encoder consists of a camera, bandwidth compression module, and a spread

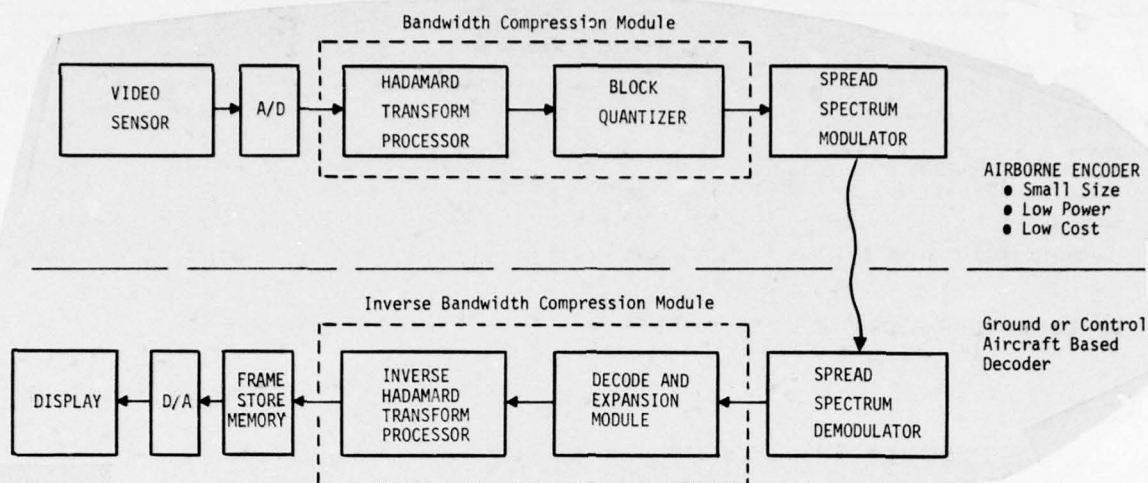


Figure 2-1. Generic Jam Resistant Video Data Link

spectrum modulator. The decoder consists of the corresponding spread spectrum demodulator, an inverse bandwidth compression module, a video refresh memory, and a video monitor. The bandwidth compression or transform encoding module consists of a Hadamard transform processor and a quantizer which is responsible for assigning more bits to the important coefficients and fewer bits to the less important coefficients. The compressed digital data is then transmitted via a spread spectrum modem implemented using a direct pseudorandom noise sequence for frequency hopping or chirp techniques. The inverse bandwidth compression module decodes, expands and performs an inverse Hadamard transform to reconstruct the compressed video signal to form a replica of the original video signal. A frame store memory is generally required at the decoder because the picture is processed in small blocks and to avoid display flicker during operational modes which require frame rate reduction. These operational modes include the standard 30 frames/sec for operation in a clear environment, selectable reduced frame rates 2, 4, and 8 frames per second, and snap shot mode for operation in heavy jamming.

2.3 SUMMARY OF RESULTS

2.3.1 Baseline Jam Resistant Video Data Transmission System

The CID focal plane processor approach offers the opportunity to relieve the size, weight, cost and power limitations imposed by the mini-RPV applications. This is accomplished by performing the transform processor function of the transform encoder directly on the image plane. As discussed in a later section, the focal plane processor can be used to implement one- and two-dimensional transform processor algorithms resulting in a significant simplification in two- and three-dimensional bandwidth compression systems. The most dramatic impact in terms of transform processor hardware savings and overall systems performance is realized in the implementation

of a hybrid interframe encoding algorithm. In this approach, a two-dimensional Hadamard transform is used to remove the spatial redundancy within a single frame while frame-to-frame redundancy is removed via a predictive coding technique, namely Differential Pulse Code Modulation (DPCM).

A functional block diagram of the system is shown in Figure 2-2. Operationally, the picture is processed in 4×4 subblocks. A two-dimensional Hadamard transformation is performed on each of the subblocks in the image plane and each of the 16 transform coefficients is encoded in the temporal direction by a bank of digital DPCM encoders. The encoded frame-to-frame transform coefficient differences are transmitted to the ground station or control aircraft over the wideband data link. At the receiver, each quantized transform coefficient is combined with its predicted value to give its reconstructed value. The 16 reconstructed transform coefficients corresponding to a particular 4×4 subblock are then sent to a digital inverse Hadamard transform processor. Since all of the transform coefficients are available and since the Hadamard transform is its own inverse, the inverse transform processor is simply a 16 point one-dimensional Hadamard transform which is implemented using standard "fast" transform algorithms similar to the FFT.

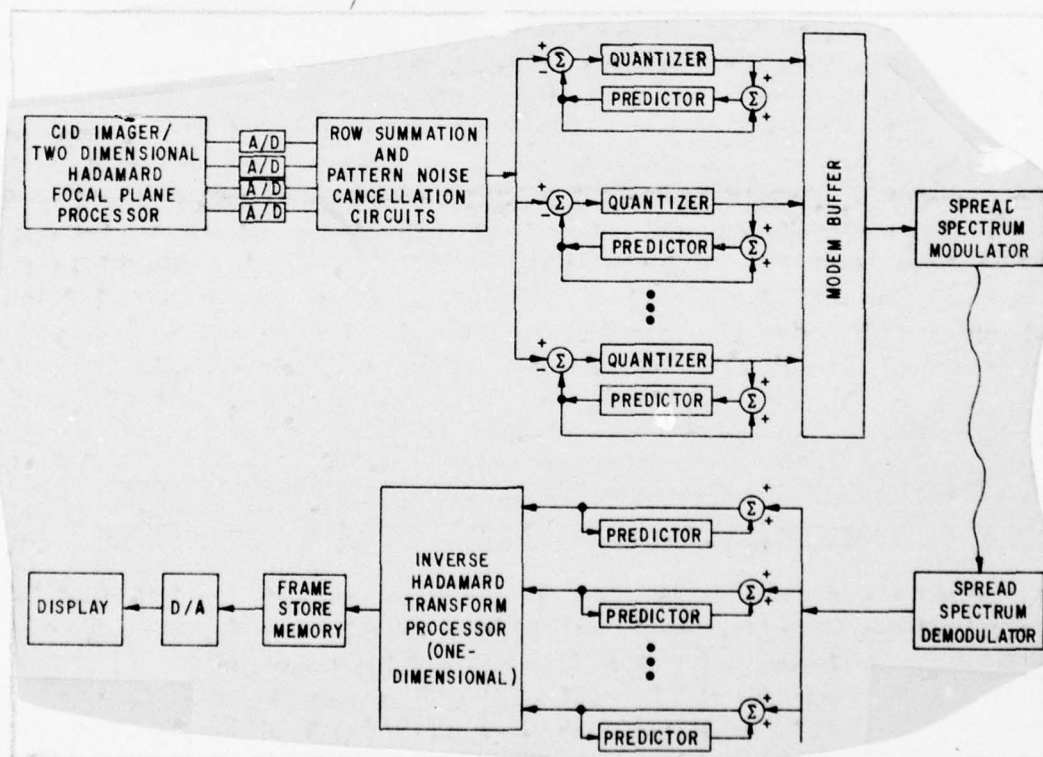


Figure 2-2. Baseline Jam Resistant Video Data Link

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The CID imager/transform signal processor and inverse Hadamard transform implementations are of particular significance to this study. The remainder of this section is directed at summarizing these implementations.

2.3.2 CID Transform Processor Implementation

Shown in Figure 2-3 are the 16 Hadamard patterns that would be applied to a 4×4 subblock of pixels. The appropriate coefficients are the sum of the applied positive and negative weighting on the intensity at each pixel. Assuming familiarity with the basic operation of the CID imager and the charge summation principle, an operational sequence for generating the 16 transform coefficients is as follows: a Hadamard code generator output is such that the array columns are driven so as to result in the application of pattern G_{00} to a particular 4×4 subblock of pixels. That is, columns 1 through 4 are driven so as to result in a positive contribution at each row output. The sum of the row 1, 2, 3 and 4 outputs gives the G_{00} Hadamard coefficient.

Notice that with no change in the column drive potentials, G_{01} can be determined directly simply by subtracting the sum of the outputs from rows 1 and 2 from the sum of rows 3 and 4. A similar observation can be made concerning coefficients G_{02} and G_{03} . The array column potentials are then driven so as to result in the application of pattern G_{10} to the 4×4 subblock of pixels. This pattern is used to generate coefficients G_{11} , G_{12} , and G_{13} . In a similar manner, patterns G_{20} and G_{30} are used to generate the remaining 8 Hadamard transform coefficients.

$G(0,0) = \begin{matrix} ++++ \\ ++++ \\ ++++ \\ ++++ \end{matrix}$	$G(0,1) = \begin{matrix} ++++ \\ ++++ \\ ---- \\ ---- \end{matrix}$	$G(0,2) = \begin{matrix} ++++ \\ ---- \\ ---- \\ ++++ \end{matrix}$	$G(0,3) = \begin{matrix} ---- \\ ---- \\ ---- \\ ---- \end{matrix}$
$G(1,0) = \begin{matrix} ++-- \\ ++-- \\ ++-- \\ ++-- \end{matrix}$	$G(1,1) = \begin{matrix} ++-- \\ ++-- \\ ---- \\ ---- \end{matrix}$	$G(1,2) = \begin{matrix} ++-- \\ ---- \\ ---- \\ ---- \end{matrix}$	$G(1,3) = \begin{matrix} ++-- \\ ---- \\ ---- \\ ---- \end{matrix}$
$G(2,0) = \begin{matrix} +--+ \\ +--+ \\ +--+ \\ +--+ \end{matrix}$	$G(2,1) = \begin{matrix} +--+ \\ +--+ \\ ---- \\ ---- \end{matrix}$	$G(2,2) = \begin{matrix} +--+ \\ ---- \\ ---- \\ ---- \end{matrix}$	$G(2,3) = \begin{matrix} +--+ \\ ---- \\ ---- \\ ---- \end{matrix}$
$G(3,0) = \begin{matrix} +-+- \\ +-+- \\ +-+- \\ +-+- \end{matrix}$	$G(3,1) = \begin{matrix} +-+- \\ +-+- \\ ---- \\ ---- \end{matrix}$	$G(3,2) = \begin{matrix} +-+- \\ ---- \\ ---- \\ ---- \end{matrix}$	$G(3,3) = \begin{matrix} +-+- \\ ---- \\ ---- \\ ---- \end{matrix}$
$G(1,0) = A+B+C+D$	$G(1,1) = A+B-C-D$	$G(1,2) = A-B-C+D$	$G(1,3) = A-B+C-D$

Figure 2-3. Two-dimensional Hadamard Patterns as Applied to a 4×4 Subblock of Pixels

Although the 4×4 Hadamard transform can be accomplished completely on a single CID focal plane processor chip, hardware implementation considerations indicate that it can best be done by designing the imager to provide four 1×4 transforms in parallel with the final row summation done digitally after A/D conversion. This issue is discussed in detail in a later section but this decision is based primarily on the following:

- A reduction in the A/D converter speed requirement allows compatibility with low cost IC circuitry.
- A reduction in the dynamic range requirement for the CID output amplifier.

An implementation of this approach is illustrated in Figures 2-4 and 2-5. The appropriate 4×4 pixel subblock is selected by selecting a particular set of four columns and four rows via the ROW SELECT and COLUMN SELECT logic. The column drive potentials are applied at the four inputs to give to the G_{00} Hadamard pattern. The sum of the four pixel values of row 1 of the subblock is available at output pad A, of row 2 at B, row 3 at C and row 4 at D. These four outputs are all that is necessary to generate the four Hadamard coefficients, G_{00} , G_{01} , G_{02} , and G_{03} . This off-chip summation is illustrated in Figure 2-5. Notice that the four coefficients are stored in a digital memory. The reason for this will be discussed shortly.

Next the column drive potentials for the selected subblock are driven to give the G_{10} pattern. The four row outputs are summed off chip in the same manner and stored. The process is repeated for the G_{20} and G_{30} patterns. At the completion of this sequence the 16 Hadamard coefficients are stored as indicated in Figure 2-5.

The coefficients are stored because they contain pattern noise. This noise is removed by injecting the 4×4 pixel block, regenerating all 16 coefficients in the identical manner in which the stored values are generated, and subtracting out the pattern noise. This technique is referred to later as "block injection."

In summary, the CID focal plane processor implementation of a two-dimensional 4×4 Hadamard transform processor has the following desirable features:

- Significant simplification in two-dimensional transform processor implementation.
- Simple Hadamard code generation since only four codes are necessary to generate all 16 transform coefficients.
- Easing of dynamic range requirements for the sense channels.
- Four-to one reduction in A/D converter speed requirement is compatible with low cost IC devices.

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Figure 2-4.
4 x 4 CID Focal Plane
Processor Mechaniza-
tion

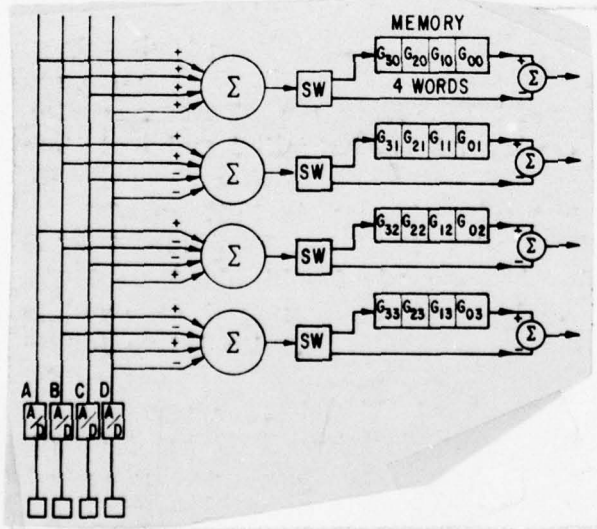
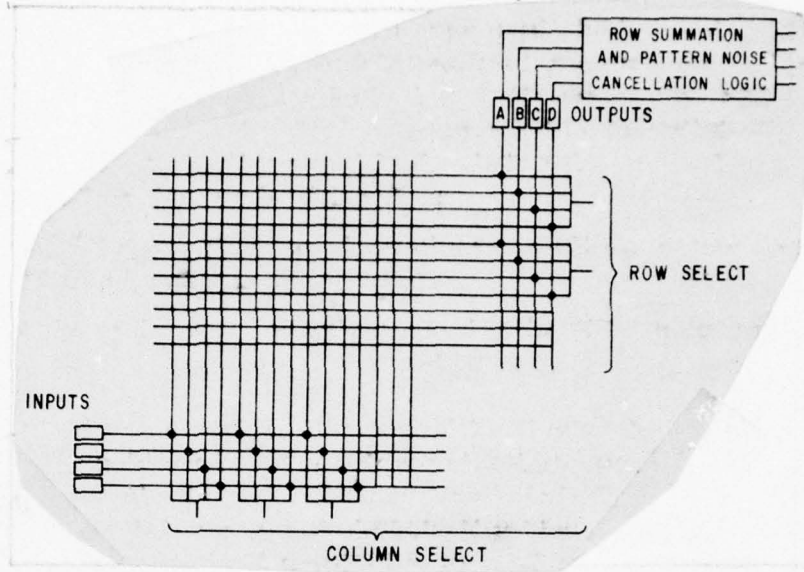


Figure 2-5.
4 x 4 Hadamard - Row Summation
and Pattern Noise Cancellation
Logic

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- Compatibility with interframe coding systems.

A variation of the above approach, described in detail in a later section, would permit the generation of an 8×8 block transformation from four 1×8 outputs. This would provide more processing gain, and near ideal theoretical coding performance at some cost in array and off-chip processing complexity.

2.3.3 Inverse Hadamard Transform Implementation

Several approaches for performing the inverse Hadamard transform were considered during the study. A trade-off of the digital implementation shown in Figure 2-6 and implementations using the General Electric proprietary SCT correlator and matrix multiplier devices clearly indicate that the digital approach is superior for this application where the size requirement of the decoder is not severe. The selection of this approach is based primarily on the fact that the data is already digital at the input to the inverse transform processor. In addition, all of the coefficient data is available for processing and two-dimensional transforms can be implemented as extended one-dimensional transforms.

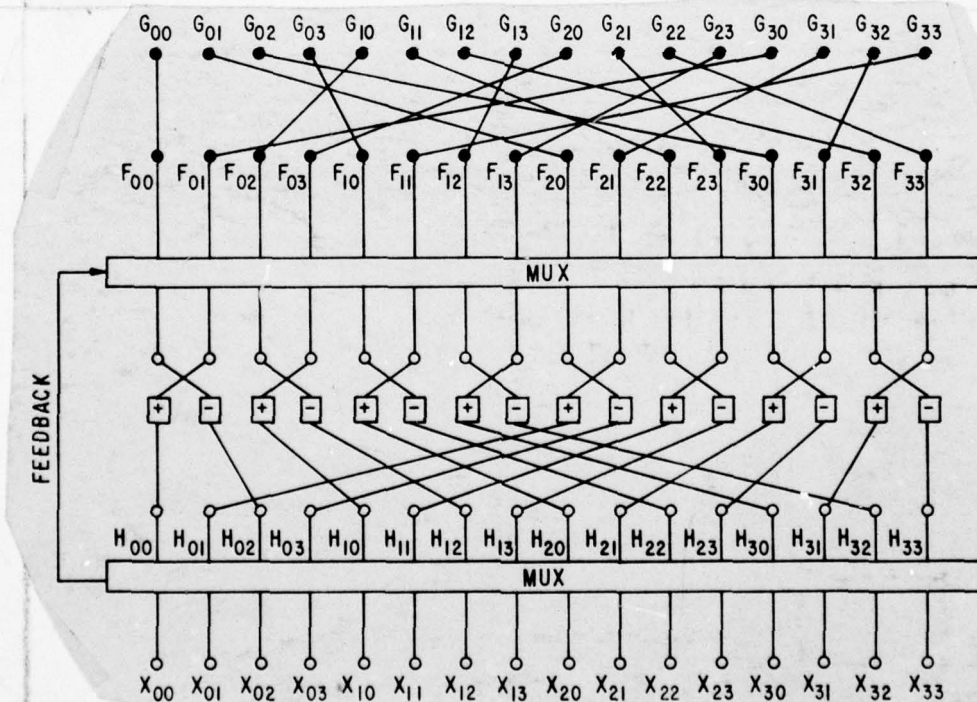


Figure 2-6. Inverse 4×4 Hadamard Transform Flow Diagram

The architecture shown in Figure 2-6 is an iterative implementation based upon a fast algorithm which gives identical stage-to-stage geometry.

This results in a hardware savings in that the hardware can be reduced to a single stage with feedback. Thus, the desired inverse transformation is accomplished after the Hadamard coefficient data is fed back four times to the input via the input multiplexer. Every fourth cycle the new transform data is entered through the input multiplexer. This data, in turn, is cycled four times during which time the previous block of pixel values are read into the frame store memory. The transform coefficients, G_{ij} , must be scrambled, as shown in Figure 2-6, prior to processing to take into account the order in which they are generated by the focal plane processor.

2.4.0 BACKGROUND

Prior to discussing implementation, it is appropriate to discuss the overall system problem to which the CID focal plane processor is being applied. A single set of system requirements does not exist at this time, making exact systems evaluation and trade-offs difficult. This section attempts to view the jam resistant video data link problem as applied to mini-RPV applications by describing the need for video bandwidth compression, briefly reviewing bandwidth compression techniques, and defining a baseline generic jam resistant video data link system. In addition to providing the background necessary to better understand what the CID focal plane processor is intended to accomplish, the subject matter contained in this section is the basis on which later sections are developed.

2.4.1 Problem Description

Jamming margin or jam resistance is the system parameter which characterizes the ability of a system to operate in a jamming environment. This parameter can be expressed as

$$M_j = G_p - [L_s + (S/N)_{out}]$$

where

M_j = Jamming margin or interference level above signal at which the system will continue to operate, i.e., jam resistance

G_p = Processing gain or signal-to-noise ratio improvement as a result of modem processing

L_s = System implementation losses

$(S/N)_{out}$ = Output information signal-to-noise-ratio

The ability of a system to resist enemy jamming, therefore, is related to processing gain which can be approximated by the ratio of RF bandwidth to information data rate. Thus, as illustrated in Figure 2-7, the task of the

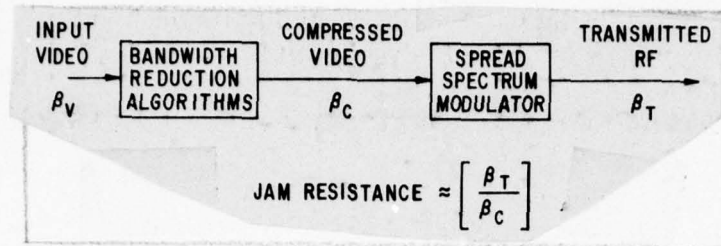


Figure 2-7. Jam Resistance Function of Airborne Encoder

mini-RPV encoder is to reduce the video bandwidth via image redundancy reduction techniques and then, using Spread Spectrum techniques, expand the compressed video signal over a wide transmitted bandwidth. The significance of bandwidth compression to video data transmission in a jamming environment is best illustrated by example. Consider a 256 line 30 frame/sec video signal that has been digitized to 6 bits per picture element (pixel), 256 pixels/line. The resultant video data rate is approximately 12 M bits/sec. Assuming 20 dB processing gain is required to achieve a desired level of jam resistance, a transmitted channel bandwidth of 1.2 GHz is required. In light of the fact that the only currently available modem for RPV applications has a bandwidth of 20 MHz, the 256 x 256 image has little chance of surviving enemy jamming.

An alternative is to reduce the bandwidth of the video by removing the natural redundancy in the image prior to transmission. The compressed video can then be recoded to fill in the allocated channel bandwidth. Computer simulations performed at the University of Southern California have shown that transform encoding, a bandwidth compression technique to be described in the next section, and frame rate control can be used to reduce the television bit rate to approximately 200 K bits/sec with only slight picture degradation. Spreading the compressed data over a 20 megabit per second channel provides the desired 20 dB processing gain.

The functional block diagram of a generic jam resistant video data link is shown in Figure 2-8. This system consists of an encoder located in the RPV and a decoder located in a control aircraft or at a ground station. The airborne encoder, consisting of a camera, a bandwidth compression module, and a spread spectrum modulator, is designed to provide the observer with the capability of varying the ratio of transmitted bandwidth to video information data rate as a function of jamming environment. The decoder consists of a spread spectrum demodulator, inverse bandwidth compression module, video refresh memory and a display. The function of the decoder is to decode the compressed transform domain video data, perform the inverse Hadamard transform and buffer the reconstructed video data so as to make it suitable for display.

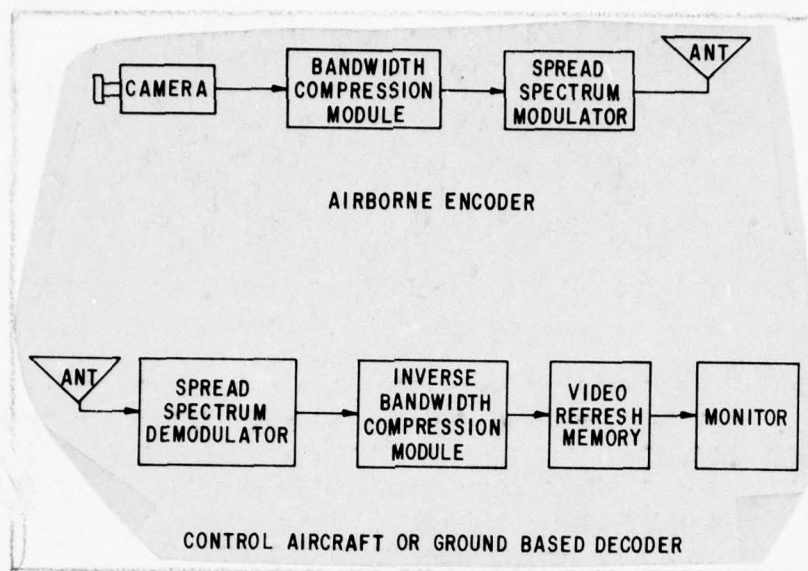


Figure 2-8. Generic Jam Resistant Video Data Link System

2.4.2 Bandwidth Reduction Techniques

As described previously, in the design of image coding systems for digital communications channels, the primary objective is to minimize the number of code bits required to reconstruct the image at the receiver. Efficient coding of the digital image is accomplished by removal of statistical redundancies that exist within the image. Transform, predictive, and hybrid transform/predictive image coding techniques have been developed to exploit intraframe spatial image redundancies.

2.4.2.1 Transform Image Coding. The basic premise of transform image coding or block quantization is that the transform domain representation of an image has an energy distribution that is more compact and therefore easier to efficiently code than the spacial domain version. Block quantization for picture data is often viewed as coding in the "frequency" domain. Since the picture data is largely low frequency, it does not utilize the total bandwidth allotted to it by resolution requirements most of the time. Thus, in the "frequency" domain the important components can be coded and the unimportant ignored or assigned fewer bits. The trivial example is that of a constant gray level which needs only one "frequency" domain component (DC component), while in the "image" domain it needs whatever the block length is. This does not imply, however, that elimination of the high frequency components is the proper choice of coding, since the human eye is more sensitive to the high frequency components. The eyes' fidelity criteria give these empirical observations a higher weight than would be given if only the standard deviation were considered. Since the image data is two-dimensional, there is correlation between lines as well as elements of one line. Therefore, the block quantization techniques can be utilized in two possible ways (Figure 2-9),

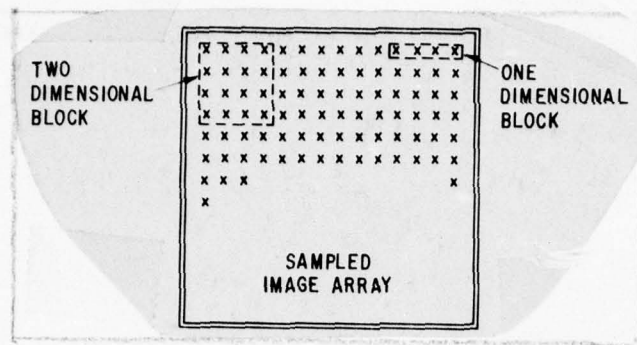


Figure 2-9. Video Block Quantization

that is, one- or two-dimensional blocks. Area transformations are attractive because they exploit correlation in both the horizontal and vertical directions but are disadvantageous in that they are difficult to implement.

In summary, then, in transform encoding systems a one- or two-dimensional linear transform of an image block is performed at the coder. The transform coefficients are quantized and coded in accordance with a predetermined bit assignment and transmitted. After decoding at the receiver, an inverse transform is taken to obtain a reconstructed image. Transforms that have proven useful for this application include Fourier, Cosine, Hadamard, Slant and Karhunen-Loeve. Simulation results indicate that a bit rate reduction to 1.5 bits/pixel can be obtained with minimal image degradation.† The bit rate can be reduced further by making the transform coding system adaptive.

2.4.2.2 Predictive Image Coding. In a differential pulse code modulation (DPCM) system, a prediction of each pixel is subtracted from its actual value and this difference is quantized and transmitted. The prediction of a data point is based upon a number of adjacent previously scanned pixel samples. DPCM works because the differential signal exhibits a significant reduction in variance as compared to the variance of the original samples. Quantization of the data is done with a quantizer designed for the probability density of the difference signal, making its performance sensitive to the statistics of the source.

Thus, the basic operation of the DPCM encoder is to generate an uncorrelated signal which is then encoded by a memoryless quantizer for transmission. At the receiver, the quantized difference signal is combined with its predicted value to form the reconstructed pixel value. Basic DPCM image

*†W. K. Pratt, "Spatial Transform Coding of Color Images," IEEE Transactions on Communication Technology, Vol. COM-19, No. 6, December 1971, pp. 980-992.

coding systems provide good quality at about 3 bits/pixel. Adaptive systems in which parameters of the quantizer and predictor adapt to image content require about 2 bits/pixel. [†]

2.4.2.3 Hybrid Image Coding^{††}. Both DPCM and transform coding techniques have been shown to exhibit some attractive characteristics and some limitations. Advantages of transform encoding system over DPCM coders include:

- Superior coding performance at lower bit rates.
- Coding degradation distributed in a manner less objectionable to a human observer.
- Less sensitivity to data statistics (picture-to-picture variation).
- Less vulnerability to channel noise.

On the other hand, DPCM systems:

- Achieve better coding performance at higher bit rates.
- Require less complex coding hardware.
- Produce a minimal coding delay.
- Do not require a large block memory.

Hybrid coding systems that combine the attractive features of transform encoding and DPCM have been investigated. Two hybrid systems have surfaced as a result of these studies. The first approach is directed at avoiding the block memory requirement of two-dimensional transform encoders while still retaining its attractive features. The hybrid encoder consists of a transform encoder in series with a DPCM filter bank. In this system a one-dimensional transform in the horizontal direction is followed by line-to-line DPCM coding of the transform coefficients. At the receiver, the transform coefficients are decoded and a replica of the original video signal is reconstructed by an inverse transform.

In the second approach, the hybrid concept is extended to interframe coding systems, that is, systems designed to make use not only of the high spatial correlation that exists within a single frame (intraframe), but also frame-to-frame correlation. In this system a two-dimensional transform is applied to each subblock. The transformed signal is then encoded in the temporal direction using a bank of DPCM encoders. Notice that this approach is similar to the first approach in that it avoids the large memory requirement associated with

[†]Pratt, op. cit.

^{††}A. Habibi, "Comparison of the n^{th} -order DPCM Encoder with Linear Transformation and Block Quantization Techniques," IEEE Transactions on Communication Technology, Vol. COM-19, No. 6, Part I, December 1971, pp. 948-956.

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performing a transform in the temporal direction in a three-dimensional encoding system.

2.5.0 GENERIC SYSTEM DESCRIPTION

Several transform encoding and hybrid coding approaches for removing video redundancy were discussed in the previous section. This section is directed at utilizing that discussion to formulate a generic baseline jam resistant video system suitable for mini-RPV applications.

The basic issue is whether the CID focal plane processor chip should be used to implement a one-dimensional transform or a two-dimensional transform on the image plane. Consider the comparison of a hybrid encoder consisting of an n^2 point, one-dimensional transform processor cascaded with a bank of n^2 DPCM encoders and a $n \times n$ two-dimensional transform encoder. Clearly, both the one- and two-dimensional transformations result in a set of n^2 coefficients each of which is a linear combination of the n^2 pixels. The difference between the two would be simply a matter of notation except when pixel subblock size and shape are considered.

2.5.1 Subblock Shape Considerations

The following considerations clearly indicate that the CID focal plane processor should be used to implement a two-dimensional transform processor:

- Two-dimensional transform encoding has exhibited better coding performance and degradation characteristics, is less sensitive to data statistics, and is less vulnerable to channel noise than the hybrid system.
- As described in Section 2-6, the CID two dimensional Hadamard transform processor implementation does not require a large block of memory as do other two-dimensional processors.
- Pixel subblock shape investigation by Wirtz† indicates that transforming two-dimensional arrays rather than one-dimensional arrays yields slightly better performance.
- A two-dimensional transform encoder allows the flexibility for extension to interframe encoding, either three-dimensional or a hybrid system consisting of a two-dimensional transform in a series with a temporal DPCM.

†P.A. Wirtz, "Transform Picture Coding," Proceedings of the IEEE, Vol. 60, No. 7, July 1972, pp. 809-819.

2.5.2 Subblock Size Considerations

Mean-square error performance improves with increasing n since the number of correlations increases with n . However, most pictures contain significant correlation between pixels for only 16 to 20 adjacent pixels.[†] In fact, in the Hadamard case a point of diminishing return is reached for $n > 8$.^{††} Even smaller n , say $n = 4$, does not significantly increase the error.

When subjective quality is the criterion, performance is essentially independent of n for $n \geq 4$.[†] Since the number of computations per pixel is proportional to n , 4×4 is a reasonable choice for picture subblock size.

Thus, depending upon the performance criterion, the optimum subblock size is 4×4 or 8×8 . The choice of 4×4 as the block size, for the jam resistant video transmission system and the CID focal plane processor chip, is based on hardware implementation considerations. As described in Section 2.6, the realization of a 4×4 CID focal plane processor is the least complex.

2.5.3 Baseline Jam Resistant Video Data Link System

Figure 2-10 shows a functional block diagram of the baseline jam resistant video transmission system. The hybrid interframe encoder is selected as baseline. Although temporal compression has no effect on the CID two-dimensional transform processor implementation, it is included to satisfy the demand for increased jamming margin in mini-RPV systems. The choice of the hybrid system over a three-dimensional transform encoder is based solely on the significant memory requirement imposed by the latter.

Referring to Figure 2-10, the picture is processed in 4×4 subblocks. A two-dimensional Hadamard transformation is performed on each of the subblocks and each of the 16 transform coefficients is encoded in the temporal direction by a bank of digital DPCM encoders. The encoded frame-to-frame transform coefficient differences are transmitted to the ground station or control aircraft over the wideband data link. At the receiver, the quantized transform coefficient is combined with its predicted value to give its reconstructed value. The 16 reconstructed transform coefficients corresponding to a particular 4×4 subblock are then sent to a digital inverse Hadamard transform processor. Since all of the transform coefficients are available, the inverse transform processor is simply a 16 point one-dimensional Hadamard transform which can be implemented using standard "fast" transform algorithms similar to the FFT.

[†]Wirtz, op. cit.

^{††}N. Ahmed, T. Natarajan, and K. R. Rao, "Discrete Cosine Transform," IEEE Transactions on Computers, Vol. C-23, No. 1, January 1974, pp. 90-93.

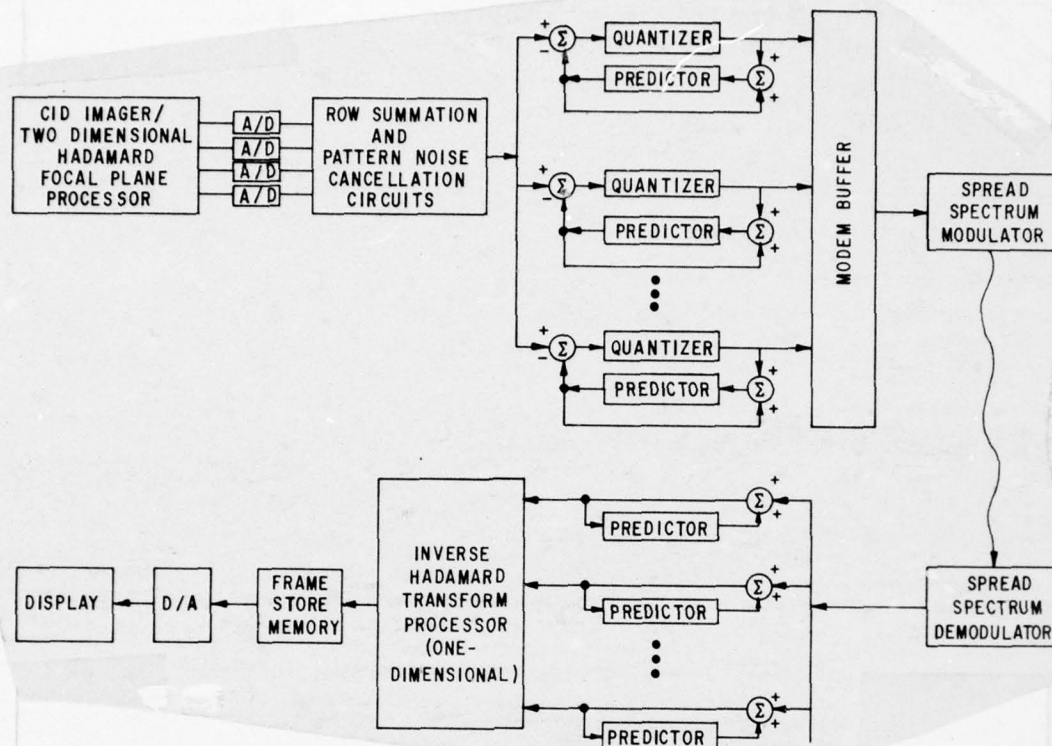


Figure 2-10. Baseline Jam Resistant Video Data Link

2.6.0 FOCAL PLANE PROCESSING

This section describes the CID focal plane processor implementation of the desired two-dimensional Hadamard transform processor. The initial discussion reviews basic CID operation and introduces the basic principles which allow the CID imager to be compatible with "on chip" one-dimensional Hadamard processing. The remainder of this section concentrates on the extension of the one-dimensional transform approach to two dimensions and the desired 4×4 Hadamard realization. In addition, a brief description of an 8×8 Hadamard implementation is given.

2.6.1 CID Imager - Operational Description

A discussion of the operation of currently configured sensors will begin based on Figure 2-11. As shown, each light-sensitive site consists of two coupled potential wells, one of which is controlled by an X, or row address, and the other by a Y, or column address. The portion of the well with the greatest depth will contain the accumulated charge. Therefore, by proper control of the address voltages, charge can be transferred between row and column segments of the site. Finally, if voltage is removed from both sections of the site, the charge will be injected into the substrate.

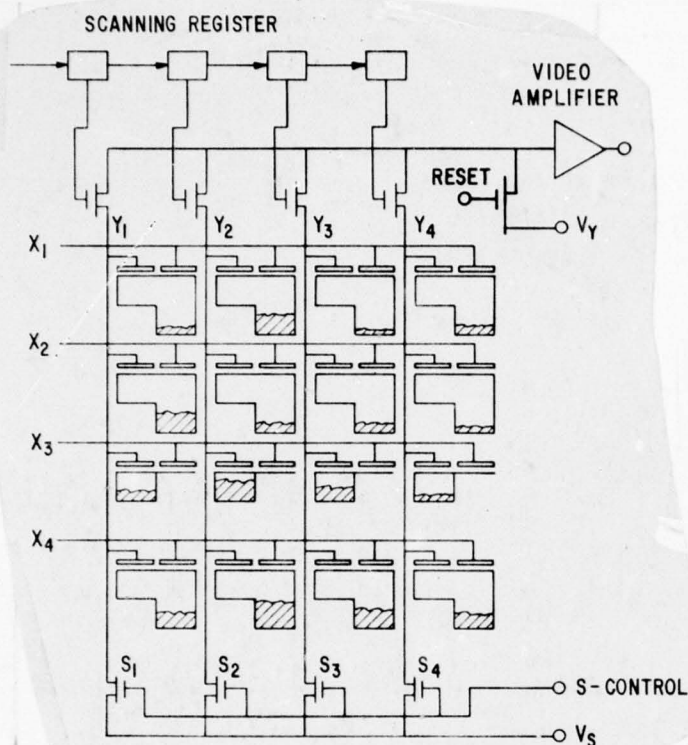


Figure 2-11.

Parallel Injection Array Diagram

Readout of such structures can be called column readout and is accomplished in the following manner. Integration of charge is done in the row potential wells. Initially, assume row X_3 is in the same mode as the other rows and that all switches are open. If the S-control switches are now closed, the column capacitances will be established at voltage V_S , after which S_1 is opened and the column lines float at V_S . Secondly, the video amplifier input line is reset to V_Y by closing the reset switch momentarily. Initial conditions are now set for signal readout. Preparation for readout of row X_3 can be made by transferring the charge under the column electrodes as shown in the figure. This, in turn, will induce a voltage change in the column lines which were left floating at V_S . Finally, readout is achieved by sequentially scanning the voltages of the column lines by closure of the switching between those lines and the video amplifier input. A reset function is performed between each column sample by closure of the reset switch, thus re-establishing the video amplifier to V_Y .

Some comments are appropriate with respect to this method of readout. It has been demonstrated successfully in operable devices; however, there are several sources of error in this technique, for which a newly conceived row readout method should provide improvement. First, the signal output is a relatively small increment which is superimposed on the value of V_Y and must be recovered external to the chip by sample and hold techniques. Secondly, the signal can be influenced by KTC effects of the three switching functions used in the readout cycle. Finally, array nonuniformities

are not suppressed. It is an awareness of these effects which led to the conception of a row readout method to be described later.

A final comment is appropriate with respect to readout. At the conclusion of the above description, the signal charge was left under the column electrodes. Several demonstrated options exist after readout. The significant aspect is that the video information has been extracted from the device without loss of the stored information. For the normal imager, the row voltage is raised and the charge is injected in preparation for the next integration period. It can, however, be transferred back under the row and retained, thus providing a nondestructive readout capability. This mode has been demonstrated where over 300,000 readout operations were conducted on a single stored image with a signal charge loss of less than two carriers per pixel, per readout.

The connotation, "parallel injection," is used to imply that injection is done for a group of sites simultaneously as opposed to a per site injection operation. Commonly, this is done for a full row during blanking time following readout of that row.

All solid state imagers (CIDs and CCDs) have been limited in dynamic range by a fixed spatial noise background caused by variations in structure and the readout process, not by temporal noise. A CID-compatible row readout method, conceived by General Electric, in principle should result in complete cancellation of these fixed pattern effects through the use of differential techniques. Additional advantages of the method are elimination of KTC effects and availability of a direct video output from the chip with associated simplification of the external video amplifier. Finally, these techniques are compatible to one-dimensional "on chip" transform processing with particular emphasis on the Hadamard transform.

One approach toward mechanizing this technique is illustrated in Figure 2-12. The vertical scanner sequentially connects on adjacent pair of row lines to the differential inputs of the video amplifier. After row selection, both lines are reset to a reference and allowed to float. The RESTORE switch is then operated to absorb the KTC offset voltage across the RESTORE capacitor. The video signal is then assembled by sequentially transferring the charge from the columns to the row electrodes. As each column transfers its charge, the amplifier output is a measure of the difference in charge transferred to the two rows. In the normal sequence one row will be empty, having just previously been cleared of signal (injected). Note that all parasitic switching effects are seen as common-mode signals by the amplifier and can be effectively rejected. The predominant source of interference is the parasitic coupling of the column drive voltage to the rows being sensed. This effect would be attenuated by the amplifier CMRR. This method measures the difference between adjacent array lines, the addressed line with signal

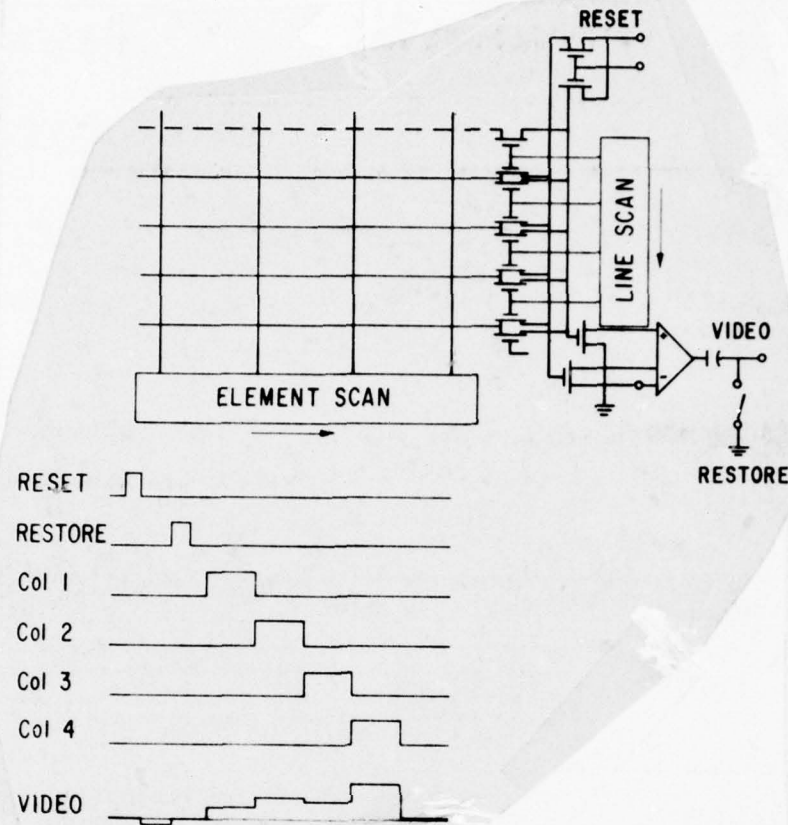


Figure 2-12. Parallel Injection Row-Readout, Differential

charge minus the previously readout line after signal charge injection. This allows cancellation of fixed pattern noise caused by column drive level differences and coarse variations in array structure. Complete cancellation could be effected by delaying the output from the addressed line for one line scan interval before subtracting the output from the empty array line. Further reduction could be effected by superimposing the rise and fall times of the column voltages; that is, have the charge transfer from the column electrode coincident with the charge being transferred out of the preceding column. Thus, the two interfering signals would tend to cancel each other. It is important to note that this scanning method forms a continuous video signal as the columns are scanned--the sampling function is inherent in the readout and need not be mechanized externally. This greatly simplifies sensing and reduces noise bandwidth. An additional advantage is the fact that the combination of injection during horizontal blanking and differential readout virtually eliminates blooming of the displayed image.

The advantages of this technique (pattern noise cancellation, KTC noise elimination, inherent signal sampling, and antiblooming) apply if the row

signals result from reading the sum of a number of image pixels as well as to the reading of a single image pixel. The method that would be used to obtain a row voltage that is proportional to the sums (and differences) of a number of image pixels is illustrated in Figure 2-13. At the beginning of a readout operation, the signal charge at some of the sites is stored under the column electrodes (q_1 and q_2) and at other locations along the same row the signal is stored under the row electrodes (q_3 and q_4). The row is reset to the reference voltage under this bias condition. If voltage is then removed from the first two column electrodes, charge packets q_1 and q_2 will transfer to the row electrodes. At the same time, voltage can be applied to the third and fourth columns causing charge packets q_3 and q_4 to transfer from the row electrodes to the column electrodes. The net change in row voltage is proportional to the sum of charge transferred ($q_1 + q_2 - q_3 - q_4$). The summation operation is controlled by the pattern of drive voltage changes applied to the column electrodes.

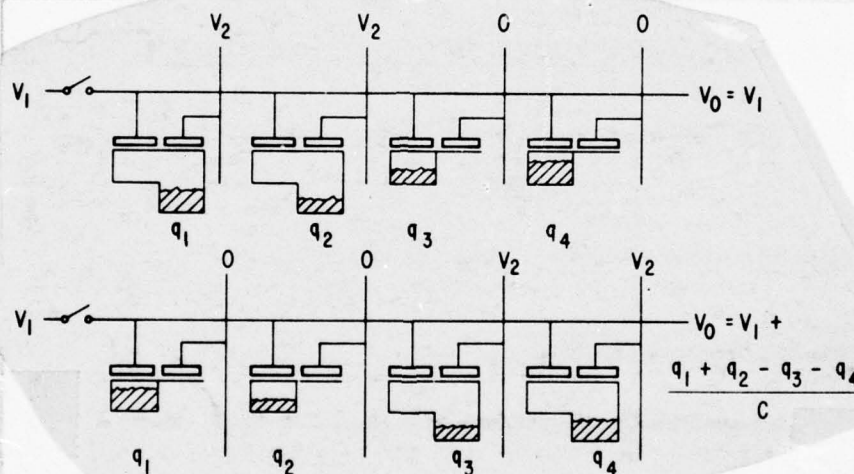


Figure 2-13. Image Plane Summation Principle

2.6.2 One-dimensional Hadamard Transform CID Focal Plane Processor

A one-dimensional Hadamard transform mechanization is as shown in Figure 2-14. The code generator is used to apply appropriate voltage changes to the column electrodes to obtain the indicated sums on the row lines. The differential row readout technique is used with this transform imager to also achieve low spatial and temporal noise. A restore operation is required between each transform point (not a reset operation). KTC noise elimination is conserved.

In the process of taking an image transform, the signal charge at each pixel is read out repeatedly, once for each transform value. For an N -wide transform, the signal recovered after taking the inverse transform is N times the signal at each pixel. The result of this repeated readout operation is a

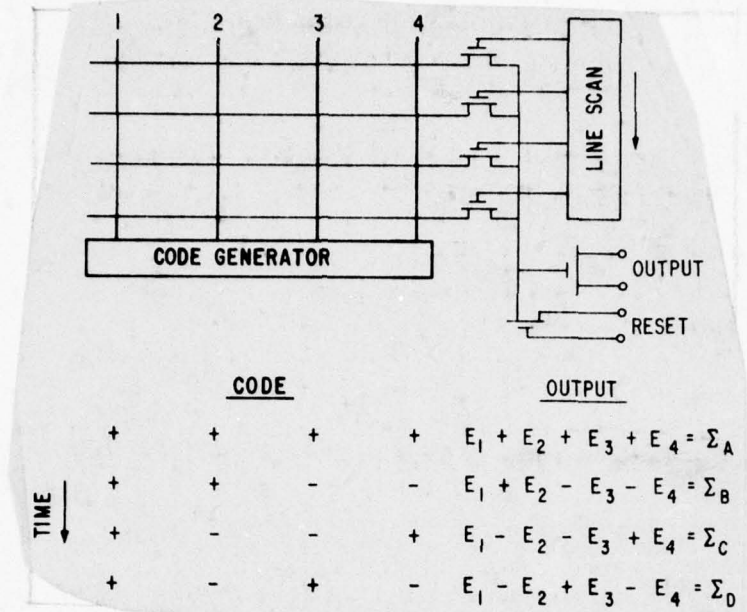


Figure 2-14. One-dimensional Hadamard Transform Implementation

signal-to-noise improvement of \sqrt{N} . Since KTC noise can be eliminated by using the row readout technique, amplifier noise will be the dominant temporal noise source. Noise levels of a few hundred carriers should be easily obtained, the specific value dependent on transform size, array size, pixel rate and amplifier design.

2.6.3 Two-dimensional Hadamard CID Focal Plane Processor

The traditional approach to taking a two-dimensional Hadamard transform is to take advantage of the separable property of the Hadamard kernel. This property allows the two-dimensional transform to be realized by taking two consecutive one-dimensional transforms. That is, a one-dimensional transform is applied to each row in the block followed by a one-dimensional transform applied to the columns of that result.

Figure 2-15 is a block diagram of an interframe encoding system using a two-dimensional transform for removing vertical and horizontal correlation within a subblock of the sampled image array. Ignoring the high speed A/D converter issue for the moment, a limitation of this approach is the auxiliary memory requirement for storing the intermediate one-dimensional transform coefficients of each block of each row. The size of this memory is significant in that it is a function of the size of the block in the vertical direction and the number of resolution elements in a row. In fact, as shown in Figure 2-15, twice this memory size is required. In light of these observations the only viable approach for implementing a two-dimensional Hadamard transform for mini-RPV applications is the CID focal plane processor.

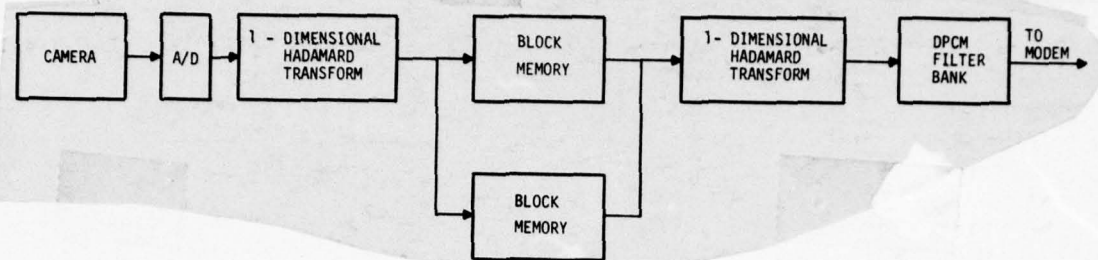


Figure 2-15. Conventional Hybrid Two-dimensional Hadamard/Frame-to-Frame DPCM Interframe Encoder

The solution to the problem of performing a two-dimensional Hadamard transform on the focal plane depends primarily on two issues:

- Column Symmetry
- Pattern Noise Cancellation

The first property is most important because if column symmetry does not exist then extending the one-dimensional concept to two dimensions is not possible. As discussed earlier, the Hadamard coefficients are generated at the row outputs by driving the array column in a prescribed manner. In other words, given a subblock size, all of the columns must have the same sign or be different by a minus sign along the row. This is illustrated in Figure 2-16. Pattern (a) is allowed because all of the elements of each column have a common sign. Pattern (b) is not allowed because columns 1 and 3 cannot be driven positive and negative simultaneously. Pattern (c) is allowed because the columns can be driven + - + - and the desired output on row 2 can be obtained by inverting the output.

+ - + -	+ - + -	+ - + -
+ - + -	- - - -	- + - +
+ - + -	+ - + -	+ - + -
+ - + -	+ - + -	+ - + -
ALLOWED	NOT ALLOWED	ALLOWED
(a)	(b)	(c)

Figure 2-16. Column Symmetry

Fortunately, column symmetry does exist. Shown in Figure 2-17 are the 16 Hadamard patterns that would be applied to a 4 x 4 subblock of pixels. The appropriate coefficients are the sum of the applied positive and negative weighting on the intensity at each pixel. Referring to Figure 2-17, notice that column symmetry exists for all 16 patterns.

$G(0,0) = \begin{matrix} ++++ \\ ++++ \\ ++++ \\ ++++ \end{matrix}$	$G(0,1) = \begin{matrix} ++++ \\ ++++ \\ ---- \\ ---- \end{matrix}$	$G(0,2) = \begin{matrix} ++++ \\ ---- \\ ---- \\ ++++ \end{matrix}$	$G(0,3) = \begin{matrix} ++++ \\ ---- \\ ---- \\ ---- \end{matrix}$
$G(1,0) = \begin{matrix} +-+- \\ +-+- \\ +-+- \\ +-+- \end{matrix}$	$G(1,1) = \begin{matrix} +-+- \\ +-+- \\ -++- \\ -++- \end{matrix}$	$G(1,2) = \begin{matrix} +-+- \\ -++- \\ -++- \\ +-+- \end{matrix}$	$G(1,3) = \begin{matrix} +-+- \\ -++- \\ -++- \\ -++- \end{matrix}$
$G(2,0) = \begin{matrix} +--+ \\ +--+ \\ +--+ \\ +--+ \end{matrix}$	$G(2,1) = \begin{matrix} +--+ \\ +--+ \\ -+-+ \\ -+-+ \end{matrix}$	$G(2,2) = \begin{matrix} +--+ \\ -+-+ \\ -+-+ \\ +--+ \end{matrix}$	$G(2,3) = \begin{matrix} +--+ \\ -+-+ \\ -+-+ \\ -+-+ \end{matrix}$
$G(3,0) = \begin{matrix} -+-+ \\ -+-+ \\ -+-+ \\ -+-+ \end{matrix}$	$G(3,1) = \begin{matrix} -+-+ \\ -+-+ \\ -++- \\ -++- \end{matrix}$	$G(3,2) = \begin{matrix} -+-+ \\ -++- \\ -++- \\ -+-+ \end{matrix}$	$G(3,3) = \begin{matrix} -+-+ \\ -++- \\ -++- \\ -+-+ \end{matrix}$
$G(1,0) = A+B+C+D$	$G(1,1) = A+B-C-D$	$G(1,2) = A-B-C+D$	$G(1,3) = A-B+C-D$

Figure 2-17. Two-dimensional Hadamard Patterns as Applied to a 4 x 4 Subblock of Pixels

An operational sequence for generating the 16 Hadamard transform coefficients is as follows. The Hadamard code generator output is such that the array columns are driven so as to result in the application of pattern G_{00} to a particular 4 x 4 subblock of pixels. That is, columns 1 through 4 are driven so as to result in a positive contribution at each row output. The sum of the row 1, 2, 3, and 4 outputs give the G_{00} coefficient. Notice that with no change in the column drive potentials, G_{01} can be determined simply by subtracting the sum of the outputs from rows 3 and 4 from the sum of rows 1 and 2. A similar observation can be made concerning coefficients G_{02} and G_{03} .

The array column potentials are then driven so as to result in the application of pattern G_{10} to the 4 x 4 pixel subblock. This pattern is used to generate coefficients G_{10} , G_{11} , and G_{12} and G_{13} . Similarly, patterns G_{20} and G_{30} are used to generate the remaining 8 Hadamard transform coefficients.

As discussed earlier, the two-dimensional Hadamard transform focal plane processor approach is not complete unless provision is made for reducing pattern noise. Two methods for achieving pattern noise cancellation are attractive, namely:

- (1) the block injection method, and
- (2) the calibrate frame method.

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In the first method the transform coefficients are generated as described above and stored. The 4×4 pixel subblock is then injected and 16 reference transform coefficients are generated on the injected block. The reference coefficients are then subtracted from the corresponding transform coefficients resulting in the cancellation of the pattern noise contained in each coefficient. The calibrate frame approach is similar to the block injection method in that pattern noise is canceled by subtracting a reference coefficient generated on an injected block from the corresponding noisy coefficient. The difference, however, is that this technique exploits the fact that pattern noise does not change appreciably with time. Thus, in the calibrate frame mode of operation, a complete single frame of reference coefficients is transmitted to the ground or control aircraft based decoder. The noisy transform coefficients are then generated as described above, transmitted, and reconstructed. The pattern noise contained in the reconstructed coefficient is canceled by subtracting the coefficient from the stored reference. This procedure is continued except that periodically (once every hour or so) the reference is updated.

An implementation of this approach, assuming the block injection method of pattern noise cancellation, is shown in Figures 2-18 and 2-19. The appropriate 4×4 pixel subblock is chosen by selecting a particular set of four columns and four rows via the ROW SELECT and COLUMN SELECT logic. The column drive potentials are applied at the four inputs to give the G_{00} Hadamard pattern, where the primed coefficients have not been corrected for pattern noise. The four row outputs available at pads A, B, C, and D are used to simultaneously generate coefficients G'_{00} , G'_{01} , G'_{02} , G'_{03} . This off-chip summation is shown in Figure 2-19. Notice that the four coefficients are stored

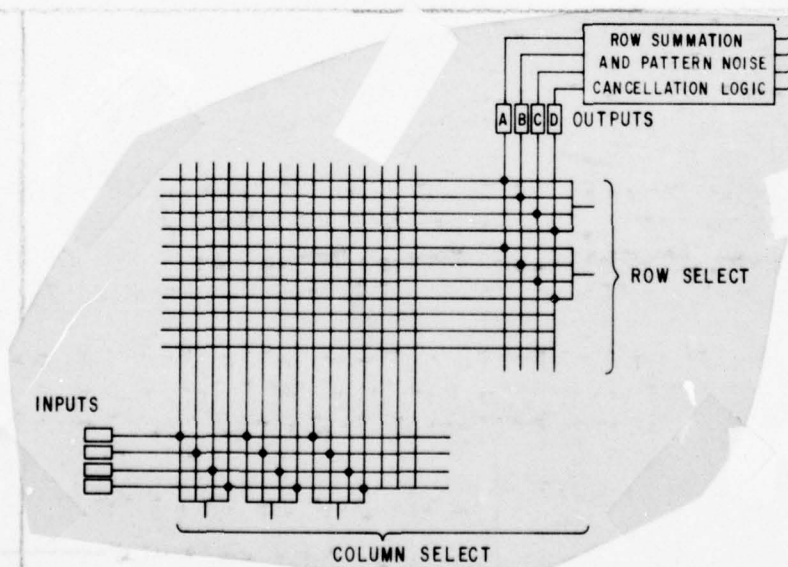


Figure 2-18. 4×4 CID Focal Plane Processor Mechanization

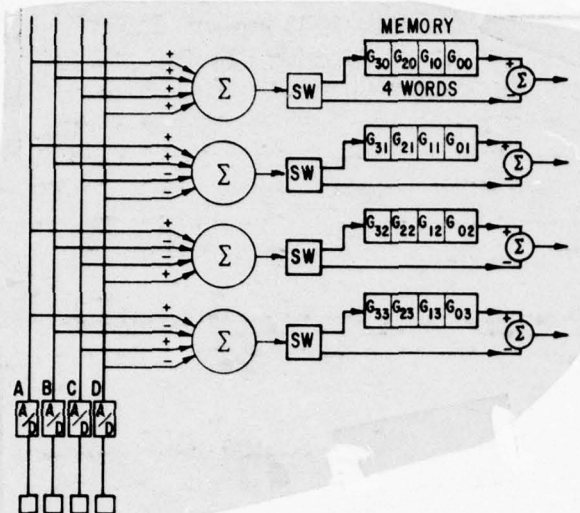


Figure 2-19. 4 x 4 Hadamard - Row Summation and Pattern Noise Cancellation Logic

in a digital memory consistent with the requirement of the block injection method of pattern noise cancellation.

Next, the column drive potentials for the selected subblock are driven to give the G'_{10} pattern. The four row outputs are summed off chip in the same manner and coefficients G'_{10} , G'_{11} , G'_{12} and G'_{13} are stored. This process is repeated for the G'_{20} and G'_{30} patterns. At the completion of this sequence the 16 noisy Hadamard coefficients are stored as shown in Figure 2-19.

The selected 4 x 4 pixel subblock is then injected and all 16 transform coefficients, G' , are generated in an identical manner over the injected subblock. As each reference coefficient, G^* , is generated it is subtracted from the corresponding coefficients and difference G is sent to the appropriate DPCM encoder for transmission. This sequence of operations is shown in Figure 2-20.

This implementation is applicable to the calibrate frame method except that the 16 memory cells are not required since the uncanceled coefficients are transmitted to the decoder where cancellation takes place. As indicated in Figure 2-21, this approach results in a four to one reduction in sample processing rate relative to the original pixel rate of the imager.

Several observations can be made concerning the implementation shown in Figures 2-18, 2-19, 2-20, and 2-21. First of all, this development is not meant to imply that the complete two-dimensional transform cannot be implemented completely on a single CID imager processor chip, because a single chip realization is possible. There are, however, advantages to designing the imager to perform four 1 x 4 transforms in parallel with the final

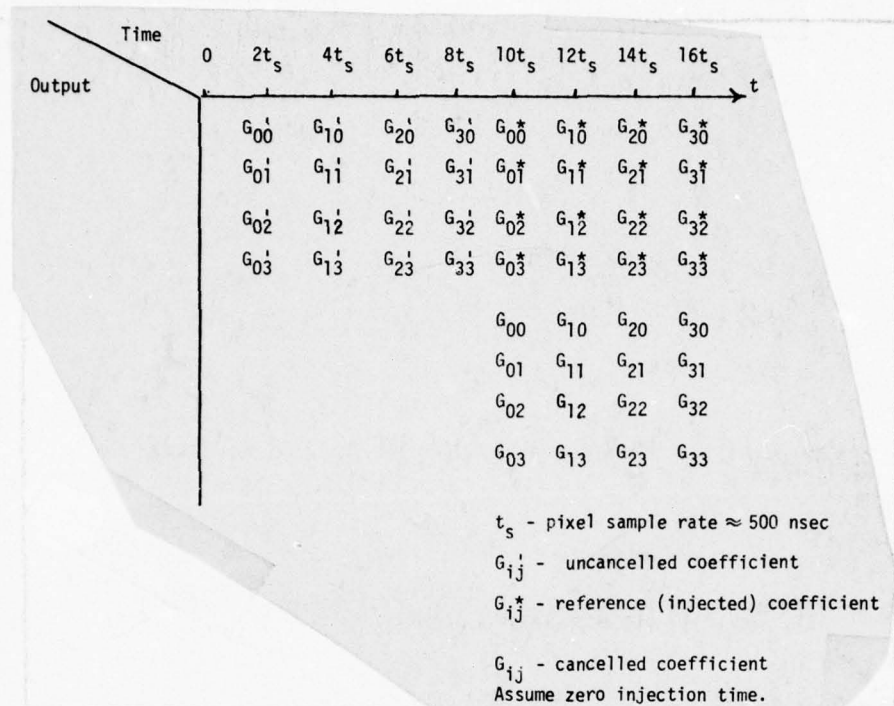


Figure 2-20. Sequence of Operations - Block Injection Method of Pattern Noise Cancellation

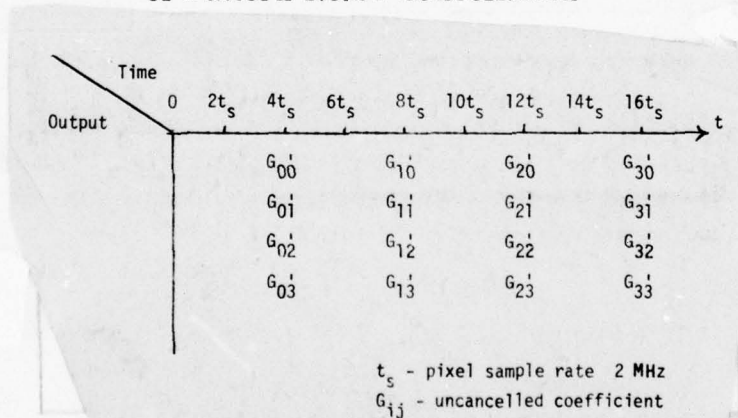


Figure 2-21. Sequence of Operations - Calibrate Frame Method of Pattern Noise Cancellation

row summation done off chip. First of all, the CID imaging chip is designed to operate at a 2 MHz sample rate. This means that a single chip implementation using the calibrate method of pattern noise cancellation would require a 2 MHz A/D converter at the input to the DPCM. If the block injection method were implemented, the A/D converter speed requirement would double. A review of A/D converter availability indicates that at 2 MHz and above either the converter is large or expensive. As shown

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in Figures 2-20 and 2-21, the parallel output implementation results in a two-to-one and a four-to-one decrease in A/D converter speed requirement. This reduction in A/D converter speed requirement allows compatibility with low cost IC circuitry and allows the CID chip to be operated at a slower rate.

A second consideration which makes the parallel implementation attractive is the dynamic range requirement for the CID output amplifier is reduced. That is, each of the four amplifiers must handle the sum of four pixel values, whereas in the single chip realization the dynamic range of the output amplifier would have to cover the sum of all 16 pixels.

2.6.3.1 An 8 x 8 Hadamard Transform Implementation on the Focal Plane. The following discussion describes an 8 x 8 two-dimensional CID focal plane Hadamard transform implementation, illustrating how the basic 4 x 4 technique can be extended to larger subpicture block sizes. There is evidence that no substantial improvement in performance is obtained for the Hadamard transform for subpicture sizes greater than 8 x 8.[†]

Figure 2-22 shows eight of the 64 possible Hadamard patterns that would be applied to an 8 x 8 subblock of picture elements. The appropriate coefficients are the sum of the negative and positive weighting on the intensity at each pixel. A CID imager chip designed to implement the 8 x 8 directly would follow an operational sequence completely analogous to that described previously concerning the 4 x 4 Hadamard implementation. A direct implementation, however, would require eight row sense amplifiers, thus presenting hardware implementation difficulties. The following paragraphs describe how an 8 x 8 Hadamard transform can be implemented using the same basic structure as the 4 x 4 chip, that is, using 4 four-input code control lines and four row outputs. The approach, therefore, is to investigate the symmetries of the 8 x 8 transform pattern, the objective being to generate 8 x 8 from two 4 x 8 transforms.

Consider first the task of driving the eight columns of the 4 x 8 block so as to apply the appropriate Hadamard pattern. Notice from Figure 2-22 that the symmetry of the generating patterns (leftmost column) is such that all that is required is that an inverter stage be added between each group of four columns. The modification to the basic 4 x 4 chip is illustrated in Figure 2-23. Notice that this minor modification allows 32 of the 64 or 1/2 of the total number of Hadamard coefficients to be generated.

The symmetry that allows the remaining 32 patterns to be calculated can be seen from the top row of 8 x 8 transform coefficient patterns in Figure 2-22. The difference between the first eight coefficients across the row and the second eight is that the lower 4 x 8 block weightings differ by a

[†]N. Ahmed, T. Natarajan, and K. R. Rao, "Discrete Cosine Transform," IEEE Transactions on Computers, Vol. C-23, No. 1, January 1974, pp. 90-93.

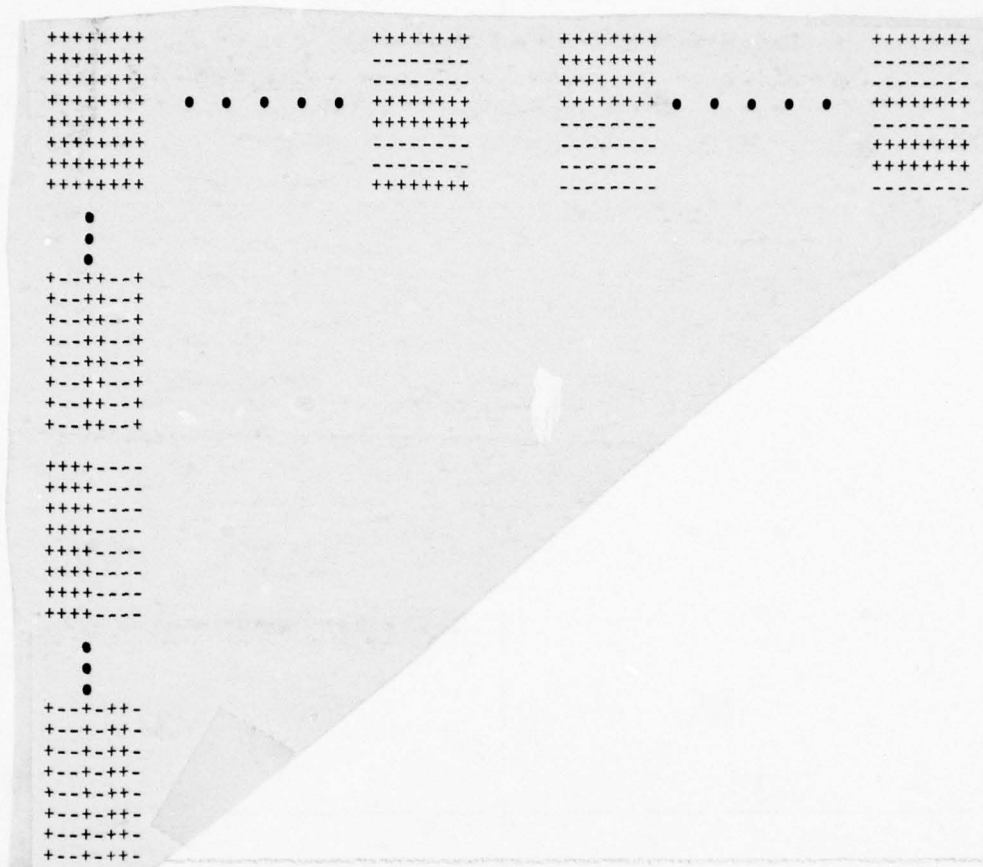


Figure 2-22. 8 x 8 Hadamard Transform Patterns

factor of -1. That is, comparing the first pattern with the fifth pattern in the top row of Figure 2-22, it is seen that the result obtained by applying the appropriate pixel pattern to the lower 4 x 8 block in the first pattern differs only in sign from the result required by the lower 4 x 8 block in the fifth pattern. Thus, the result need only be calculated once.

The operational sequence is to select the upper 4 x 8 of the 8 x 8 subblock by addressing the appropriate ROW SELECT lines. Eight columns are selected by addressing the appropriate two adjacent COLUMN SELECT lines. With the inverter control off, an all-positive pattern is applied at the input resulting in a 4 x 8 block of positive pixel weightings. The four partial Hadamard transform coefficients are calculated and stored in the same manner as described in the 4 x 4 implementation. In fact, as shown in Figure 2-24, the off-chip row summation logic is identical. Now, without changing the input pattern, the appropriate inverters are turned "on" resulting in the application of the fifth pattern in the leftmost column (see Figure 2-22) to the same upper 4 x 8 pixel subblock. The four partial Hadamard results are generated in the same manner. This procedure is continued until all 32 unique upper 4 x 8 results are obtained and stored.

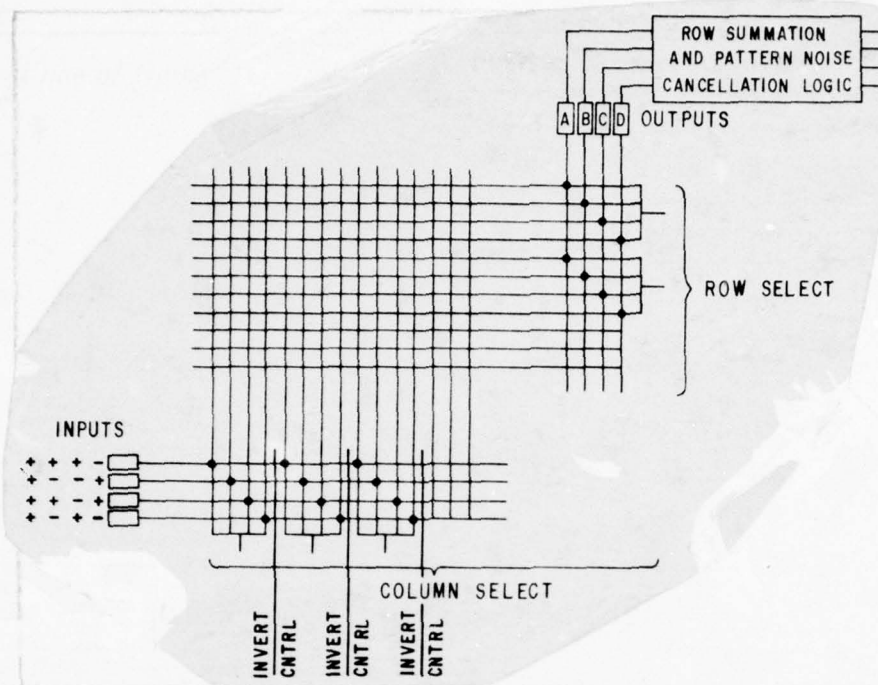


Figure 2-23. 8 x 8 CID Focal Plane Processor Mechanization

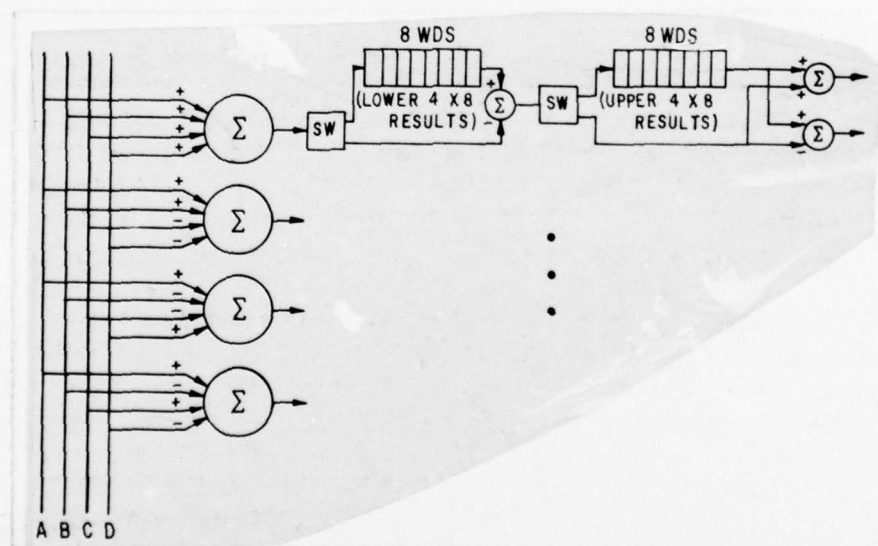


Figure 2-24. 8 x 8 Hadamard Transform - Row Summation and Pattern Noise Cancellation Logic

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The upper 4×8 is then injected and the 32 required reference values are generated and pattern noise cancellation is achieved as shown in Figure 2-24.

The lower 4×8 block is then addressed via the ROW SELECT logic and the identical procedure is followed for generating the 32 pattern noise-free results. At this point in the sequence the upper and lower results corresponding to the first four columns (32 coefficients) in Figure 2-22 are stored. As shown in Figure 2-24, all 64 coefficients are then generated by adding and subtracting the lower 4×8 results from the upper 4×8 results.

In summary, it is possible to perform FFT type operations on the focal plane to realize larger subblock transforms. The 8×8 subblock transform provides more processing gain and near theoretical coding performance at the same expense in array and off-chip complexity.

2.7.0 INVERSE HADAMARD TRANSFORM APPROACHES

Several approaches for performing the inverse Hadamard transform were considered during the study. A digital iterative implementation is compared to two sampled analog implementations using the General Electric proprietary SCT correlator and matrix multiplier devices, a comparison which indicates that the digital approach is superior. The major reason is that the data is digital at the input to the inverse transform processor.

The three approaches are described in the following paragraphs. It should be noted that all three implementations take advantage of the fact that all of the coefficient data are available for processing and the 4×4 inverse Hadamard transform can be implemented as a 16 point one-dimensional transform.

2.7.1 SCT Correlator Implementation

The SCT correlator[†] is a surface charge device capable of correlating an analog waveform with a digital reference. This is a very powerful signal processing technique because it performs parallel analog summation operations under digital control at high data rates. A correlator structure with parallel digital input capability is diagrammed in Figure 2-25. The inverse transform operation would be mechanized by loading the 16 two-dimensional transform coefficients into analog storage and then successively applying the 16 Hadamard binary patterns to the digital inputs. A correlator would be the preferred approach for performing the inverse transform function for a wide transform; however, its use does not appear to be justified for this particular application for two reasons. First, the transform coefficients

[†]J.J. Tiemann, W.E. Engeler, and R.D. Baertsch, "A Surface Charge Correlator," IEEE Journal of Solid State Circuits, Vol. SC-9, No. 6, December 1974, pp. 403-410.

are available from the data link in digital form and the frame store memory would most likely be digital. The use of a correlator would require D/A conversion prior to the inverse transform operation, and A/D conversion following that operation. Secondly, the size of the inverse transform computation, 16 additions/subtractions, is small enough to be easily mechanized in digital form with existing MSI circuitry.

2.7.2 Matrix Multiplier Implementation

A family of CCD matrix multiplier chips is currently under development at the General Electric Company's Research and Development Center. This family is being developed to eliminate the complicated peripheral circuitry of previously considered CCD transform signal processing approaches. In addition, the signal processing operations are all performed in parallel so that extremely high speeds (complete transform in 100 nano-seconds) are possible. The family will require essentially no clock drivers, and output circuits are all on chip. The basic multiplier module will be 16 x 16 elements and will perform the mathematical operation

$$\begin{bmatrix} V_{out(1)} \\ V_{out(2)} \\ \vdots \\ V_{out(16)} \end{bmatrix} = \begin{bmatrix} W_{1,1} & W_{1,2} & \dots & W_{1,16} \\ W_{2,1} & \dots & \dots & \dots \\ \vdots & \vdots & \vdots & \vdots \\ \dots & \dots & \dots & W_{16,16} \end{bmatrix} \begin{bmatrix} V_{in}^{(1)} \\ V_{in}^{(2)} \\ \vdots \\ V_{in}^{(16)} \end{bmatrix}$$

That is, a column vector of input voltages will be multiplied by a matrix of fixed weights (on chip) to yield a column vector of output voltages simultaneously (see Figure 2-26). For this application the weights W_{ij} are the appropriate 1 and -1 weights required by the inverse Hadamard transform.

The comments concerning the suitability of the SCT correlator approach also apply to the matrix multiplier approach.

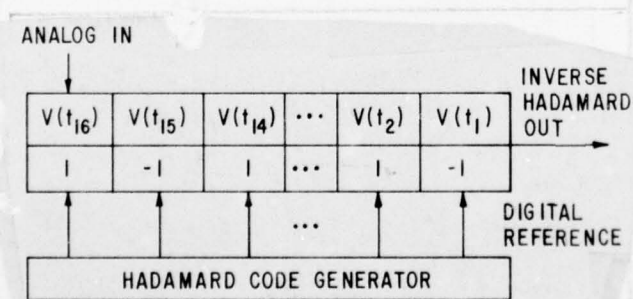


Figure 2-25. Modified SCT Correlator

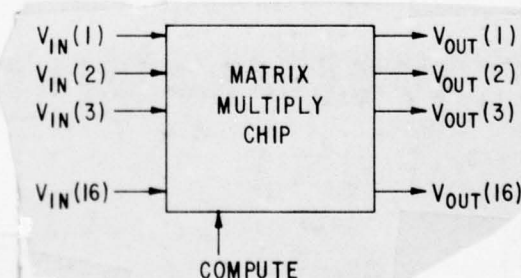


Figure 2-26. Basic Matrix Multiply Chip

2.7.3 Digital Iterative Implementation

Figure 2-27 shows an iterative implementation based upon a fast algorithm which gives identical stage-to-stage geometry. This results in a hardware savings in that the hardware can be reduced to a single stage with feedback. Thus the desired inverse transform is accomplished after the Hadamard coefficient data are fed back to the input via the input multiplexer four times. Every fourth cycle the new transform data are entered through the input multiplexer. These data, in turn, are cycled four times during which time the previous block of fixed values are read into the frame store memory. The transform coefficients, G_{ij} , must be scrambled, as shown in Figure 2-27, prior to processing to take into account the order in which they are generated by the focal plane processor.

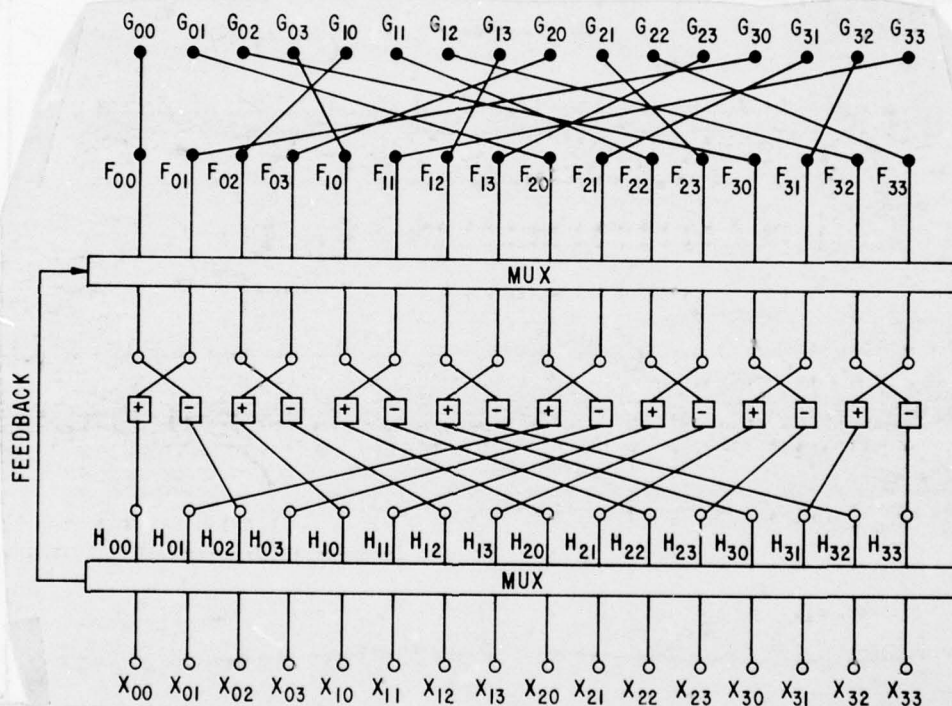


Figure 2-27. Inverse 4 x 4 Hadamard Transform Flow Diagram

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3.0 SYSTEM DESCRIPTION

3.1 CID ARRAY DESIGN

3.1.1 Cell Layout

Figure 3-1 shows the 1.2×1.2 mil cell layout of the 128×128 sensor. The thick-thin oxide boundary is dashed, the lower conductor (N-doped polysilicon) crosshatched, and the upper level (N-doped polysilicon) conductor is shown in solid outline. The lower level poly-thin oxide capacitor has an area of 0.21 mil^2 and the upper level poly-thin oxide capacitor has an area of 0.28 mil^2 . Since the upper level capacitor has a thicker dielectric than the lower level capacitor, the charge storage capacity of each electrode is approximately the same, 1.9×10^6 carriers. Depletion capacitance loading limits the maximum output charge to 1.5×10^6 carriers.

Both levels of N-doped polysilicon conductors have a sheet resistivity of approximately 10Ω per square. An alternative approach is to substitute metal-oxide for the polysilicon on the upper level. This would result in higher sensitivity since the metal-oxide is highly transparent.

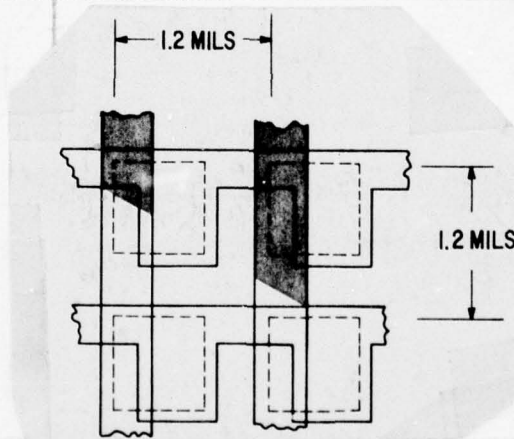


Figure 3-1. Cell Layout

3.1.2 Array Layout

The array (Figure 3-2) contains 128 rows and 128 columns, selected by groups of four on both the horizontal and vertical axes. Since this array was designed for sequential readout of the image subblocks, selection is by means of scanning registers. In operation, a logical "one" would be entered into each scanning register and shifted as required to select the desired subgroup. The column drive lines, E_1 through E_4 , would then be driven to obtain four transform outputs in parallel.

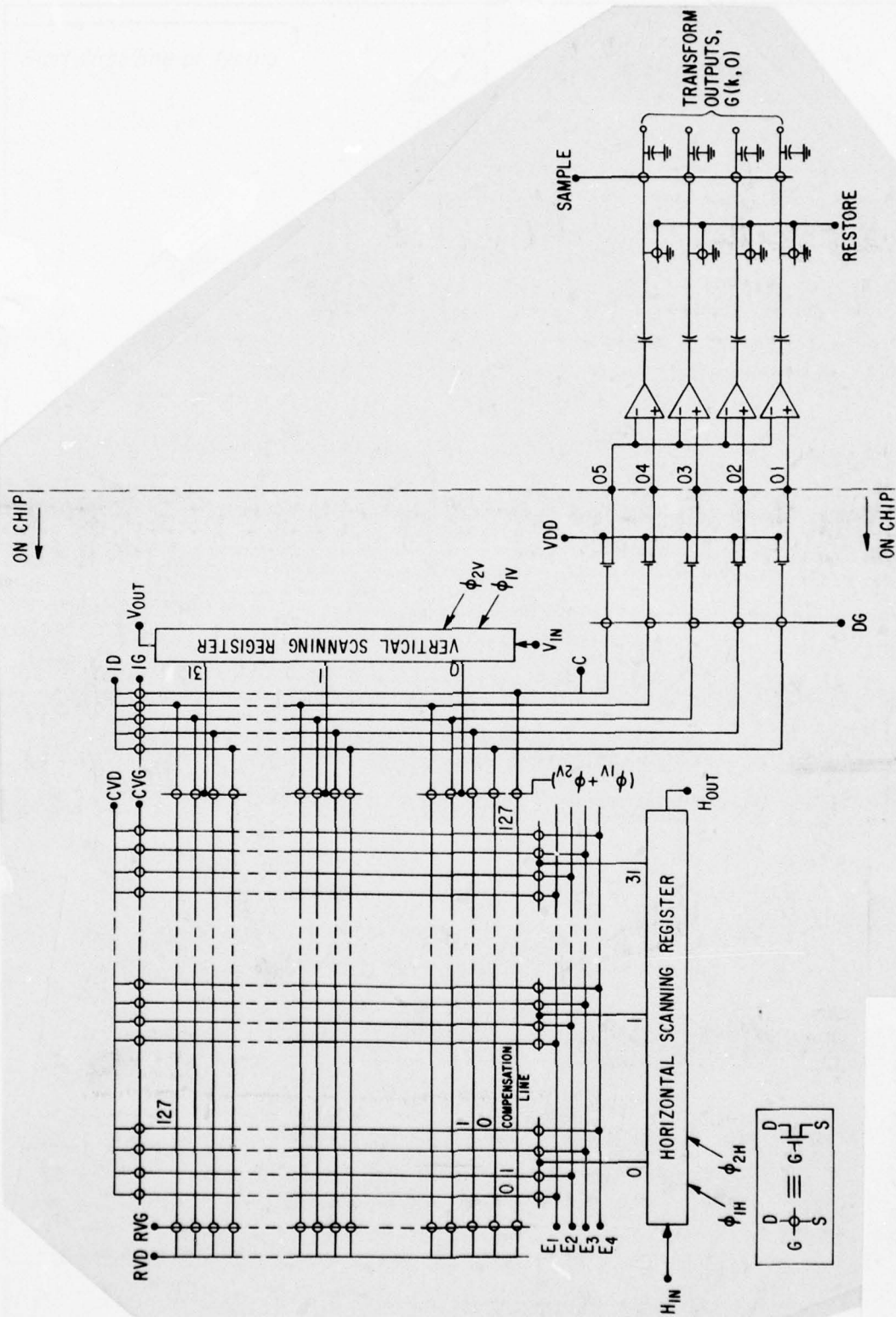


Figure 3-2. Sensor Layout

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In addition to the 128 active rows, an additional row is available to provide differential cancellation of column drive interference. This compensation row is selected for every row address and cleared when every row is cleared.

The five on-chip MOSFET preamplifiers, shown at the lower right of Figure 3-2, are optional. By means of photo-mask selection, these devices can be bypassed should off-chip preamplification be desired.

Site size is 1.2×1.2 mils, giving an active sensing area of 153.6×153.6 mils. Overall chip size is approximately 200×200 mils (5×5 mm).

3.1.3 Array Parameters

The calculated array electrical parameters for the 128×128 format are shown in Table 3-1.

Table 3-1
ELECTRICAL PARAMETERS

Cell Storage Capacity	1.9×10^6
Saturation Output Charge	1.5×10^6 (.24 pC)
Distributed Row Capacitance (C_{ROW})	6 pF
Sense Line Capacitance (C_S)	12 pF
Distributed Row Resistance	3.9 K
Row Select Transistor Resistance	4K

3.2.0 SYSTEM LOGIC AND TIMING

The timing diagram for transform readout shown in Figure 3-3 is generated by the logic diagram shown in Figure 3-4. Block 1 is a voltage controlled oscillator which has two clock outputs, one fixed and one variable. Block 2 switches between the two clocks. The outputs of counter 3 are the clock frequency divided by 2 and divided by 8. Gates 4-8 select which of the two frequencies to be fed into counter 9. Its outputs are used as inputs for the PROM. The PROMs are 32 words of 8 bits each. The switching of counter frequencies allows generation of the first 16 words at low frequency and the second 16 words at high frequency, thus allowing more precise placement of the signals for injection, reset, etc.

One of the PROM outputs is a pulse labeled ϕ . The rising edge of this pulse turns off a phase line and the falling edge of the pulse turns on the other phase line. This is done by using the pulse as the clock input to a positive

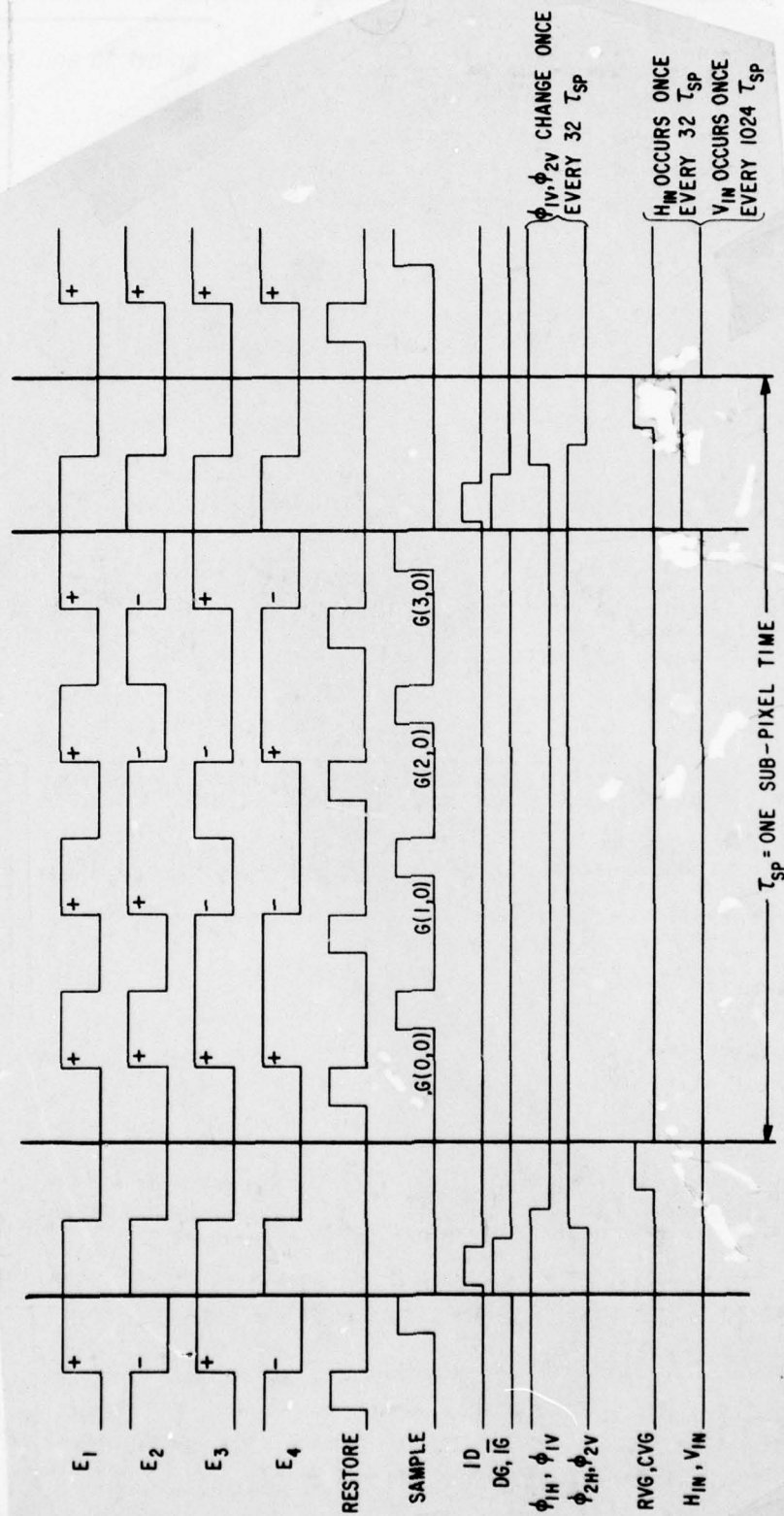


Figure 3-3. Timing Diagram for Transform Readout

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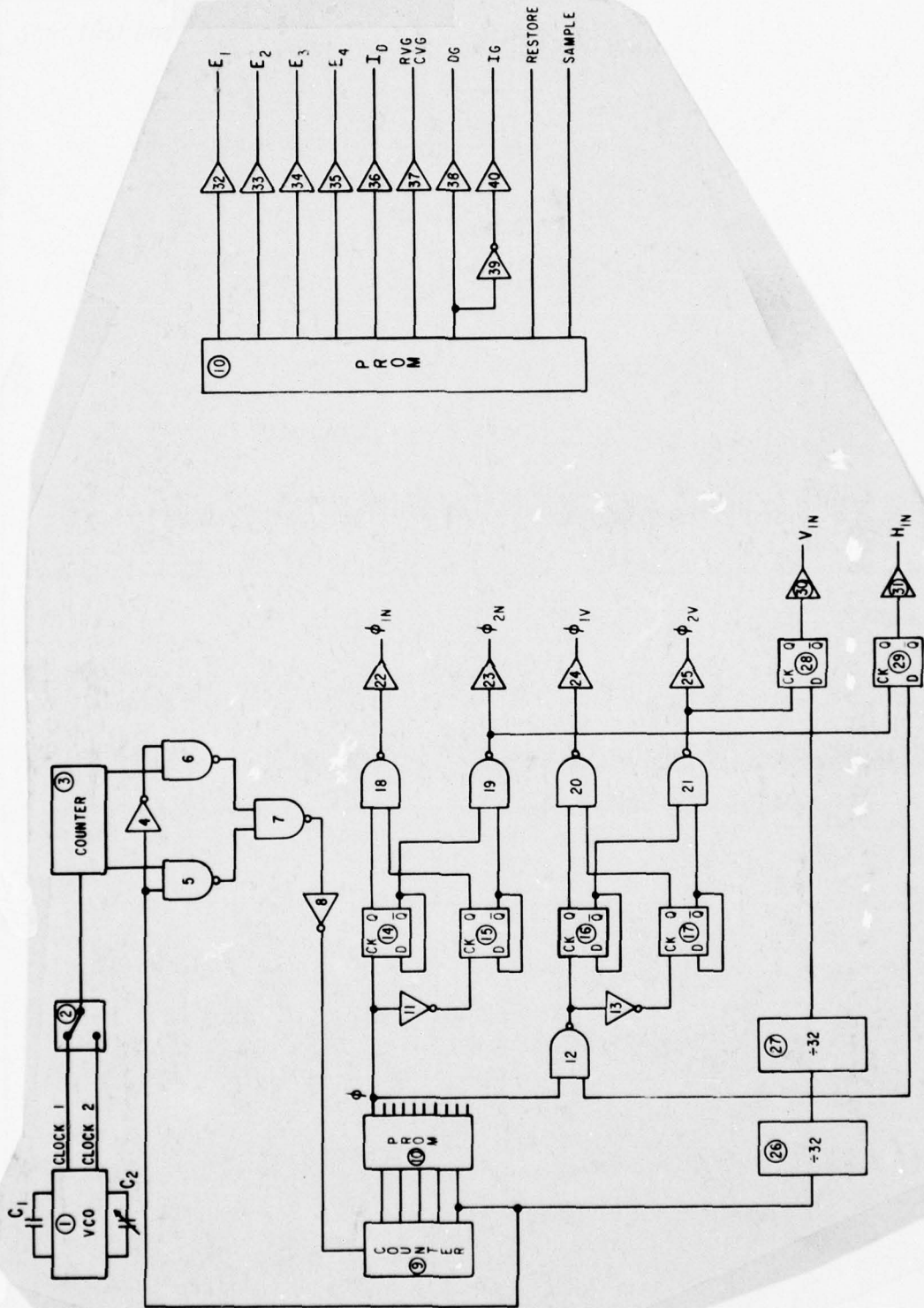


Figure 3-4. Logic Diagram for Transform Readout

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edge-triggered flip-flop (14), while inverting the pulse and using it as the clock input to another positive edge-triggered flip-flop (15). Both noninverted outputs are NANDed, giving ϕ_1 , while the inverted outputs are NANDed, giving ϕ_2 . Blocks 22, 23 are drivers as are blocks 24, 25, 30-38, and 40, thus providing the required voltage levels needed for the chip.

The counter 9 output, which cycles once every PROM interval, is divided by 32 to give one pulse every line. This is NANDed with the ϕ signal. Then ϕ_{1V} and ϕ_{2V} are generated the same way as ϕ_{in} and ϕ_{2H} . The once-a-line pulse is also used to generate H_{in} . When ϕ_{2H} turns off while the once a line pulse is on, the output of flip-flop 30 turns on. The next time that ϕ_{2H} turns off, the once-a-line pulse is off, so the flip-flop output is off. The flip-flop's inverted output is then used as H_{in} . The once-a-line pulse is divided by 32, to give a pulse once every frame. This signal is used to generate V_{in} in the same way as H_{in} was generated.

All the other necessary signals are from PROM outputs driven by 32 through 38 and 40, to give the necessary levels. RESTORE and SAMPLE are sent directly to switches on the sense amplifier side of the camera.

The assembled transform readout camera board is shown in Figure 3-5. Logic, timing, and drive circuits are to the left of the 28 PIN imager package (center white ceramic package), and the four video amplifiers to the right.

Logic and timing diagrams for the normal readout camera are shown in Figure 3-6 and Figure 3-7, respectively.

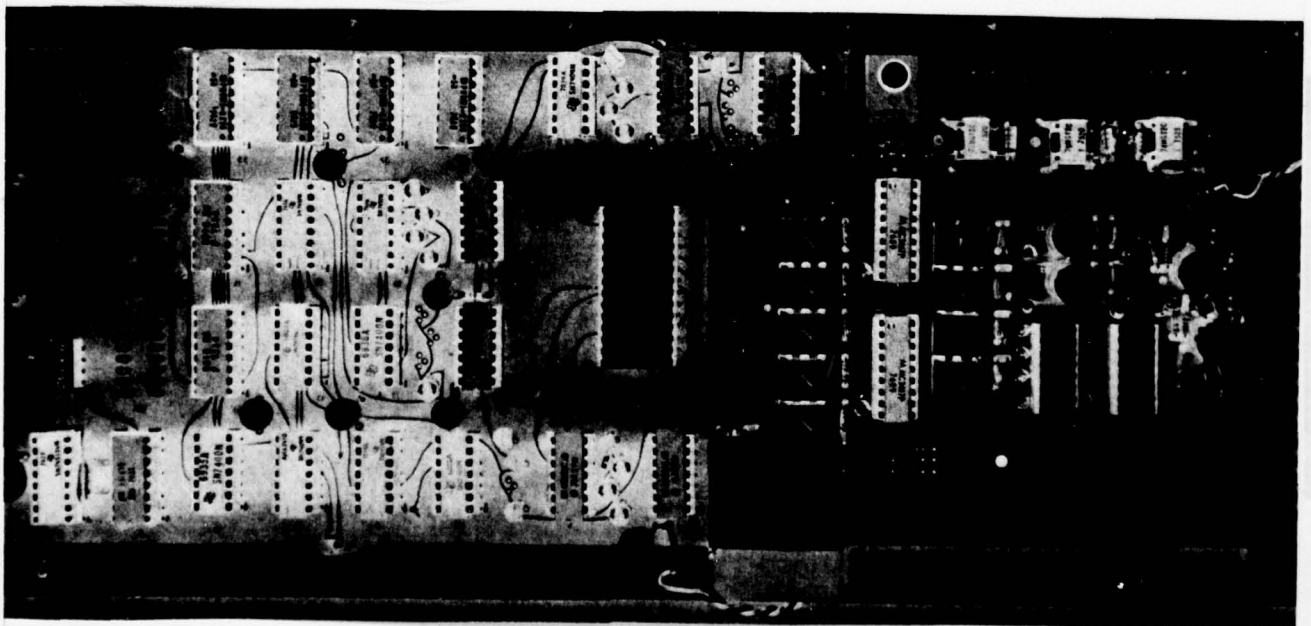


Figure 3-5. Camera Circuit Board

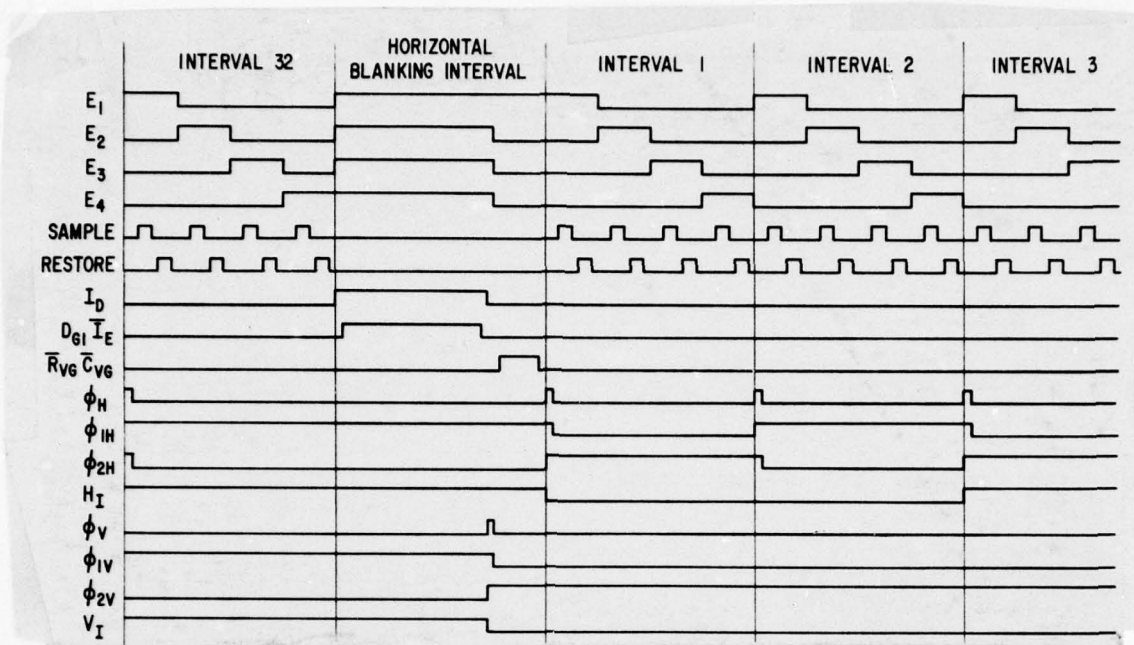


Figure 3-7. Timing Diagram for Normal Readout

3.3.0 VIDEO SIGNAL RECOVERY

The four parallel video amplifier channels have been shown in functional diagram form in Figure 3-2. During readout a 4×4 subblock is selected, 4 columns by the horizontal scanning register, and 4 rows by the vertical scanning register. A compensation row is always selected to allow the column drive voltage, which couples to the row conductors, to be cancelled by the differential amplifiers.

The readout sequence then proceeds as follows:

1. All rows are reset to a reference voltage, RVD, and allowed to float.
2. The KTC offset noise is removed by operating the RESTORE switches to acquire samples of the offset voltages across the restore capacitors.
3. The column conductors are driven through connections E_1 , E_2 , E_3 , and E_4 either in a time sequential (Normal Readout) or Walsh code (Transform Readout) manner to transfer signal charge to and from the row electrodes. The restore switches are operated between each column drive voltage change to provide the proper zero reference.
4. After all data from either the addressed block (Transform Readout) or addressed rows (Normal Readout) has been read out, that section of the array is cleared of signal charge by driving the injection transistors (I_G & I_D) and the appropriate column conductors to cause signal injection. The video amplifiers would be disconnected during the injection operation by switching off gate DG.

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A detailed schematic diagram of one of the four identical readout amplifiers is shown in Figure 3-8.

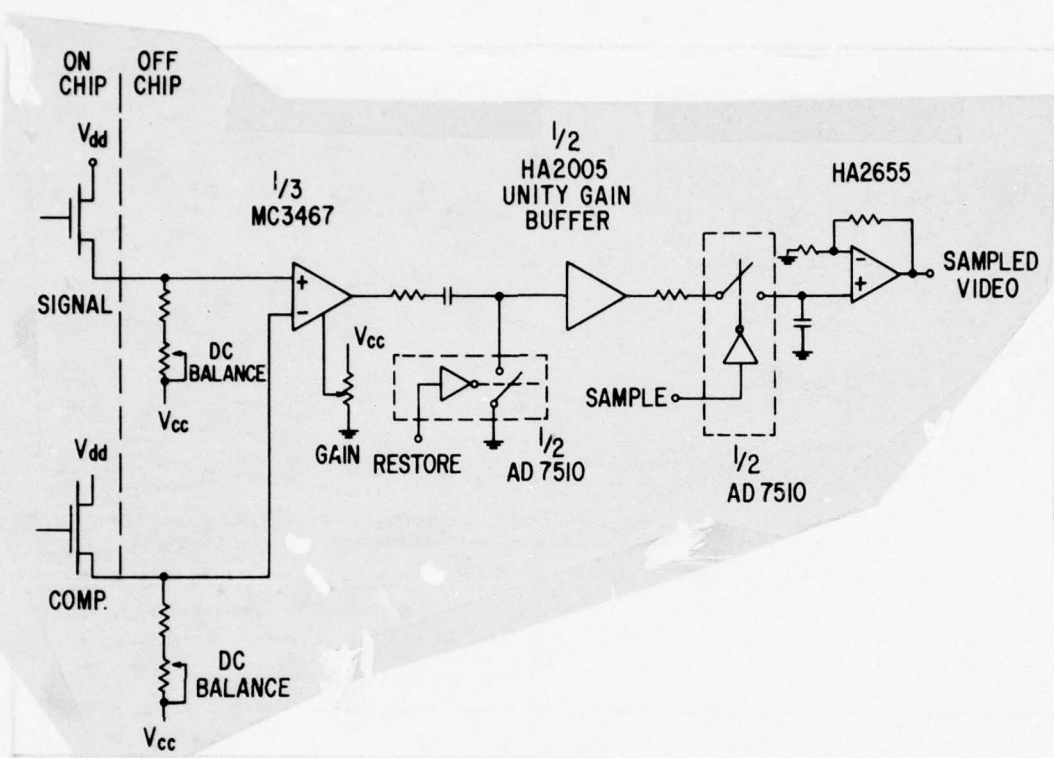


Figure 3-8. Video Amplifier Schematic

4.0 FABRICATION PROCESS

The CID Processor chips were fabricated using the P-channel overlapping electrode process with both the lower and upper electrodes formed from N-type polysilicon layers. This process has been developed particularly for the fabrication of solid-state imagers and incorporates many safeguards to maintain a reasonably high yield even with large chip size.

For the subject devices we were able to obtain a functional yield of 87% and a line defect-free yield of 21% using high-quality, hard material masks. These results are outstanding considering that the chip size is 190 x 210 mils, larger than most memory or microprocessor chips. A photo of the array is presented in Figure 4-1. A detailed distribution of defects among the various elements of the array is shown in Table 4-1.

Table 4-1
PROCESSING RESULTS

Wafer No.	No. of Chips	Functional	Defects				Defect Free	Defect Free & Low Dark Content
			Row	Column	Vertical Register	Horizontal Register		
1	56	52	16	29	2	1	13	5
2	56	50	20	22	1	1	13	9
3	56	46	23	11	1	7	13	6
4	56	50	14	28	3	3	12	3
5	56	47	18	17	4	1	14	11
6	56	48	13	25	9	2	7	3
Total	336	293	104	132	20	15	72	37
%	100	87	31	39	6	4	21	11

The starting material consisted of epitaxial silicon wafers, with the substrate heavily doped with boron; the epitaxial layer was phosphorus-doped with a resistivity of 10 Ω -cm. The thickness of the epitaxial layer was approximately 25 μ m.

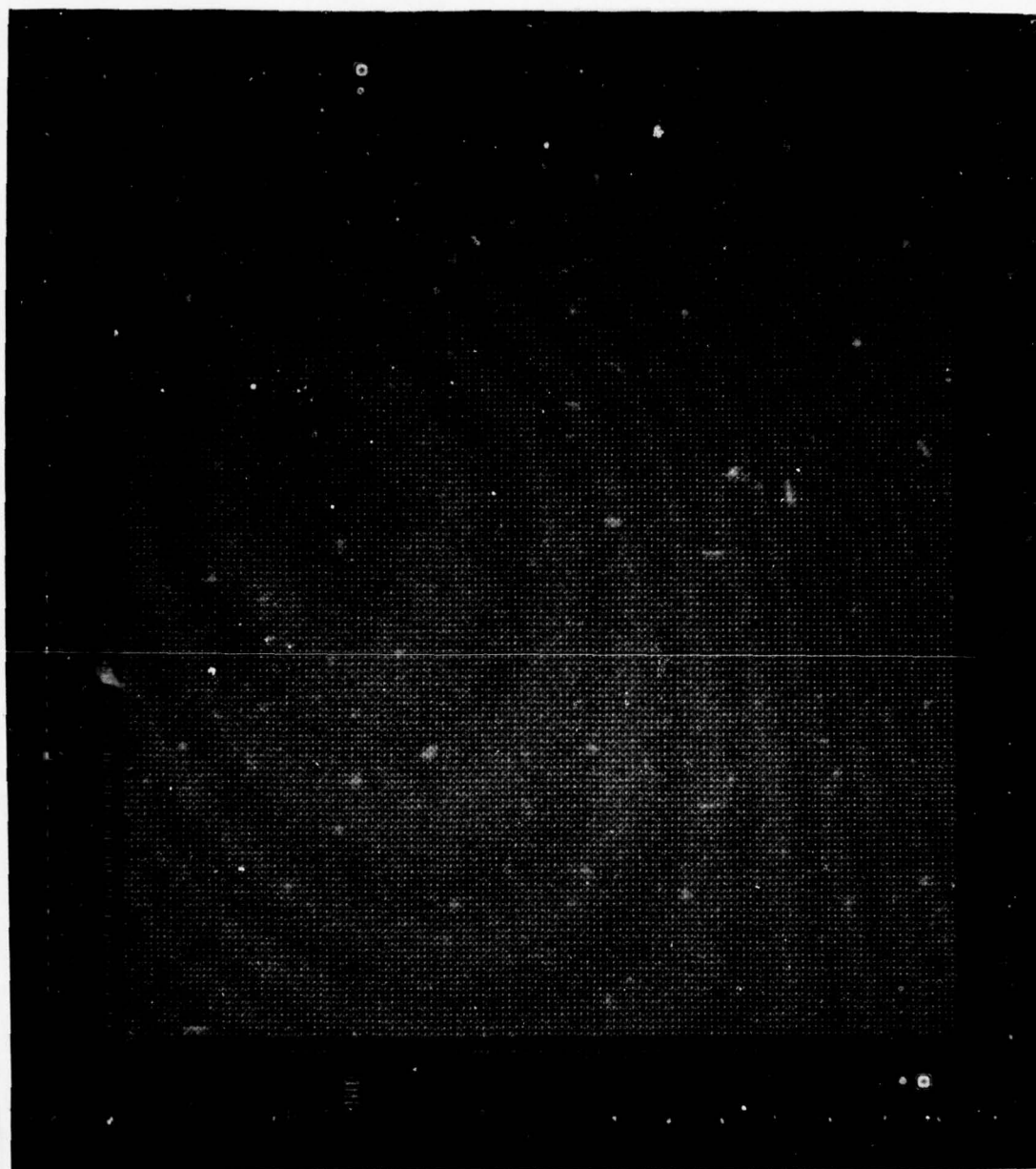


Figure 4-1. Chip Photomicrograph

The field oxide is partially countersunk into the silicon surface for eliminating large and abrupt steps at the edges of the active regions. This allows the use of thicker field oxides, providing higher field threshold voltages (~ 30 V @ $1\mu\text{a}$) and lower parasitic capacitance (~ 0.018 pF/mil²).

The lower level electrode is made of chemical vapor-deposited polysilicon, which is then phosphorus-doped to increase its electrical conductivity. A sheet resistance of about $10\ \Omega$ per square was measured on a

Nicholson/BB 4-3

polysilicon layer 5000 Å thick. A gettering process is coupled to polysilicon doping for improving the imagers' dark current characteristics.

The polysilicon lines are selectively passivated by growing about 3000 Å of oxide in steam. Thus the interlevel capacitance is only 0.016 pF/mil². By comparison, the polysilicon electrodes' capacitance in the active regions is 0.26 pF/mil² with a threshold voltage of -1.6 V. A second level of polysilicon was used for the upper electrode, but it did not extend to the scanning registers section. The top metallization in the scanning registers was aluminum evaporated from an induction-heated crucible.

Three lots, of 6 wafers each, were processed for this program. In the first two lots we used emulsion photomasks since hard material ones were not readily available. Yield was very low in these early lots, particularly in the shift registers. In the course of the failure analysis we were able to correlate this yield loss to a geometrical distortion of the emulsion masks, known as the Ross effect.[†] Basically, this is due to the difference in drying rates between exposed and unexposed gelatin during development of emulsion photomasks. Shrinking of the dark regions by as much as 0.05 mils at each edge is often observed. In our case, the failure occurred when a polysilicon line overlying a field oxide strip, designed to be 0.1 mil wider at each edge, turned out to be coincident, because of the concomitance of the Ross effect in the polysilicon and field oxide patterns. The aluminum lines could not cross this enhanced step and broke frequently, decreasing the yield.

With the introduction of hard material masks this problem disappeared and the high yield of the third lot, previously mentioned, was observed.

1900. Vol. 52, 98 (1920).

[†]F. E. Ross, Astrophysical Journal, Vol. 52, 98 (1920).

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5.0 PERFORMANCE

The CID processor arrays were tested in both the normal mode (sequential scan) and the transform mode. Experimental results are tabulated and compared to the specifications.

5.1 IMAGER PERFORMANCE - NORMAL READOUT

A series of eight packaged arrays from the third lot was tested in the normal-readout camera. Nondestructive readout was verified on all of them, as the camera was set up for multiple frame integration. In this mode the charge could be injected after n frames where n could be varied from 1 to 1000. Other device characteristics for the series are shown in Table 5-1. All values are for a readout rate of 30 frames/second. The gain factors used for these calculations are based on capacitance measurements and are derived in Appendix B.

The experimental measurements were made using the data collection system shown in Figure 5-1. The heart of the system is a microcomputer, consisting of an Intel 8080 processor and 24 kilobytes of user-accessible memory. A 12-bit A/D converter along with timing logic is used to convert the video signal into digital form for input to the microcomputer where it is processed under software control. A teletype and control panel are used to control the data collection. This system was used to measure the following characteristics.

5.1.1 Dynamic Range

Dynamic Range was measured by first taking 100 readings with no illumination. Then 100 readings were taken under full-scale illumination and the mean value of the background subtracted from each reading. The dynamic range was the average value of these 100 readings of the signal-minus-background, divided by the standard deviation of those readings (the RMS noise level). The light source used was a tungsten point arc lamp.

The dynamic range measured was about 500:1 for all arrays. This was achieved with the on-chip signal attenuation of 2:1 ahead of the amplifiers as described in Appendix B. If the layout error responsible for this signal attenuation were corrected, a dynamic range of 1000:1 would be achieved.

5.1.2 Dark Current

The dark current levels were measured using the multiple frame integration feature of the camera. Dark current buildup was measured after 200 and 300 frames of integration. The background levels were quite low, allowing about 17 seconds to reach saturation at 25 °C, equivalent to about 500:1 peak signal to average dark current ratio, although all of the arrays

Table 5-1
DEVICE CHARACTERISTICS

Device Number	Dynamic Range	Dark Current nA/cm ²	Sensitivity a/w
3-5-44	523:1	1.06	.14
3-5-31	504:1	1.25	.15
3-5-30	494:1	1.20	.14
3-5-28	568:1	0.82	.16
3-5-20	534:1	1.06	.14
3-3-46	547:1	1.11	.17
3-3-40	513:1	1.06	.16
3-3-28	528:1	0.82	.15

had a few dark current "spikes." The variation in the background dark current level between arrays is partially due to the variation in temperature of the arrays. Chip temperature increased by approximately 15°C during operation. This variation can be reduced by decreasing the power dissipated by the on-chip preamplifiers.

5.1.3 Spectral Response

A representative spectral response (Figure 5-2) was taken on an array from lot 2 using a calibrated monochrometer. The peak quantum efficiency (45%) occurs at a wavelength of .66 μ m. This series of devices was tested for response at this wavelength using a collimated light source and narrow band interference filter. A United Detector Technology calibrated silicon photodetector was used as a reference. The results are tabulated in Table 5-1.

5.1.4 MTF

Data was taken on the arrays to determine a point spread function, using a 0.1 mil light spot from the tungsten arc lamp. The light spot was moved along a row and column in 1/10 element-width increments. These results are shown in Figures 5-3 and 5-4. The transfer function was measured using a series of neutral density filters. This is shown in Figure 5-5.

5.1.5 Uniformity

Pixel-to-pixel background variations (fixed-pattern noise) were measured by first taking the mean of 25 readings at each of 50 sites along an unilluminated row. This was to reduce temporal noise. The 49 differences between

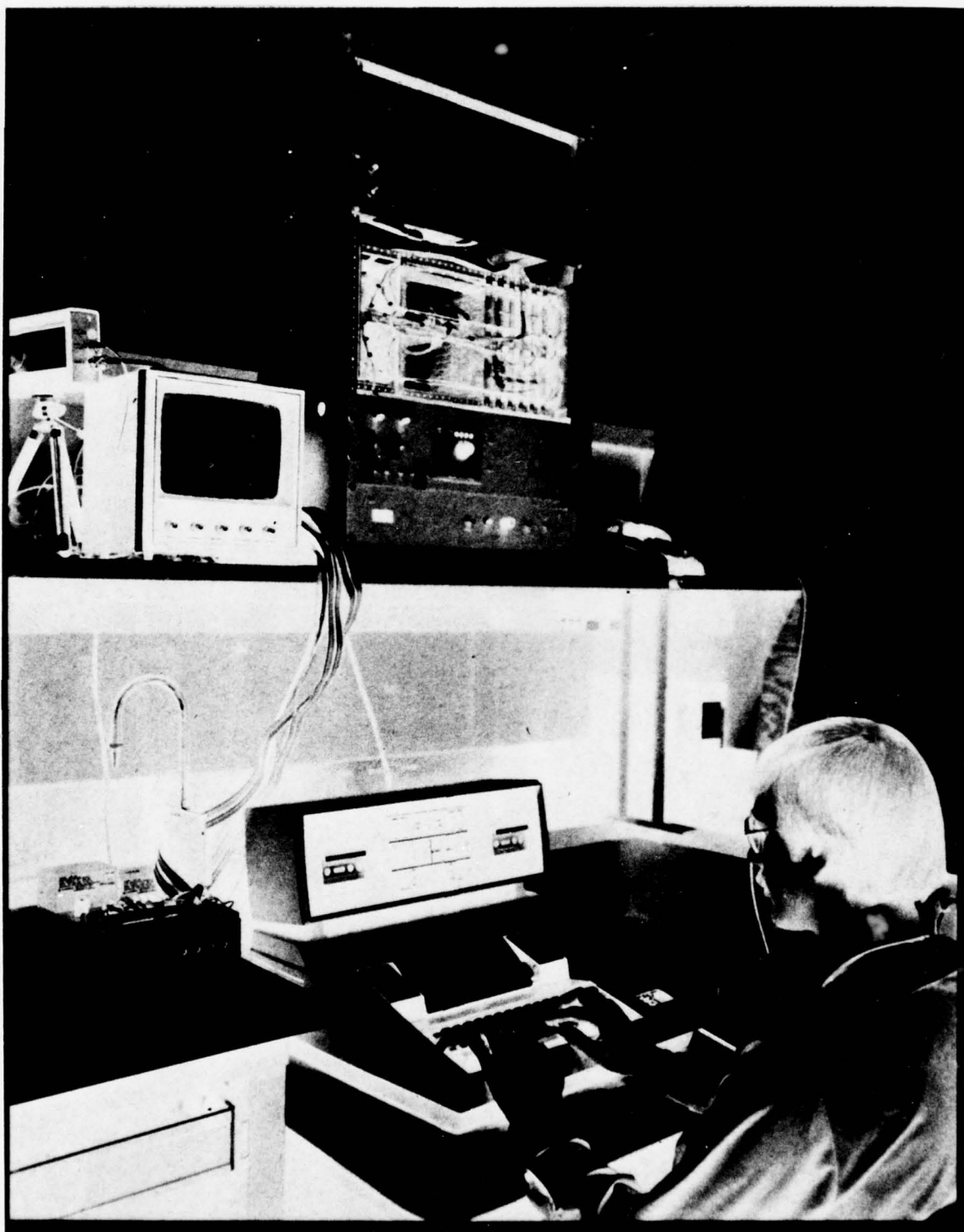


Figure 5-1. Data Collection System

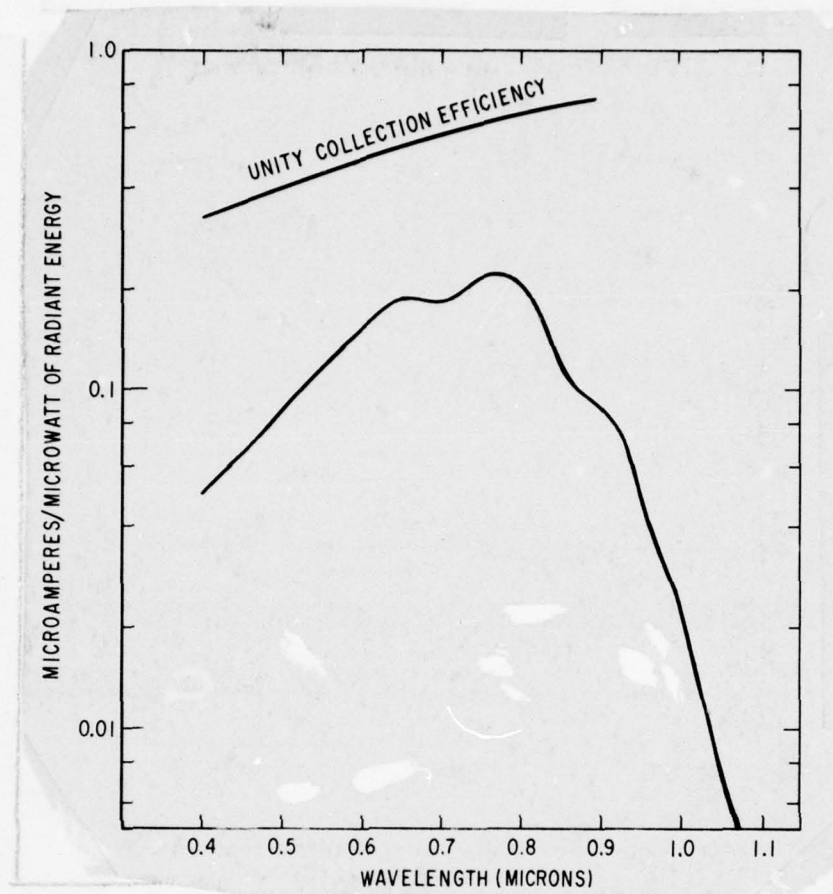


Figure 5-2. Spectral Response

the mean background values for adjacent sites along the row were then summed and divided by 49 to determine the average pixel-to-pixel background variation. Typical results are shown in Figure 5-6.

The decrease in fixed-pattern noise with increasing row number is attributed to increasing effectiveness of the compensation row, which is Row 128.

Pixel-to-pixel sensitivity variations were measured by first finding the mean signal (25 readings) for 3/4-full scale illumination, minus the mean signal (25 readings), for no illumination, at each of 50 sites along a row. The 49 differences of these signal-minus-background values for adjacent sites were then averaged to determine the pixel-to-pixel sensitivity variation. Figure 5-7 shows that the variation in sensitivity is less than the background variations, and does not vary significantly across the array.

5.1.6 Qualitative Performance

A photograph of the monitor display produced by a typical imager operating in the normal readout mode is shown in Figure 5-8. A few bright defects

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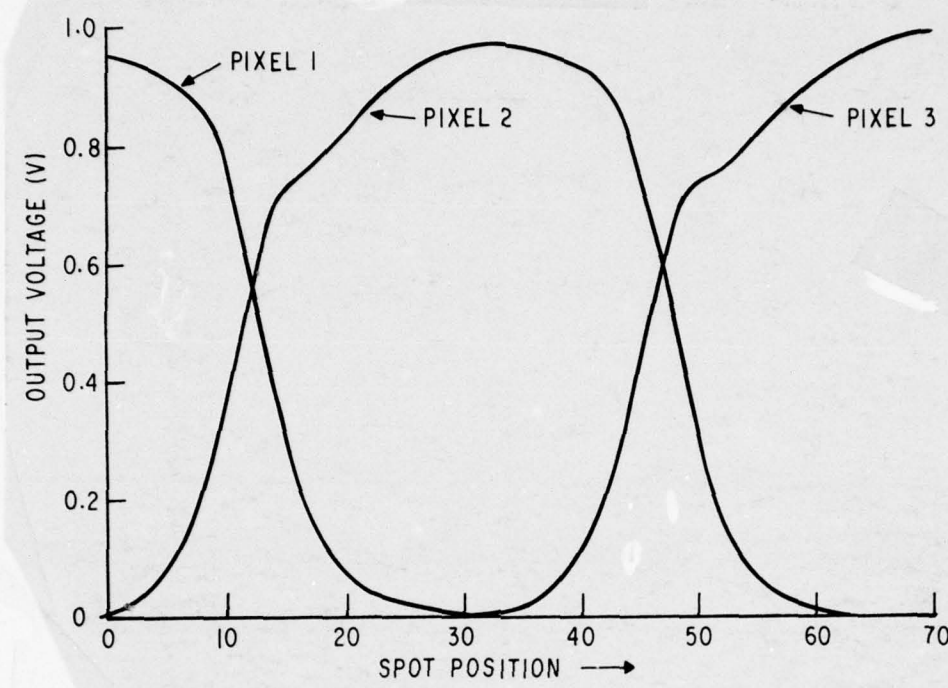


Figure 5-3. Point Spread Function, Horizontal

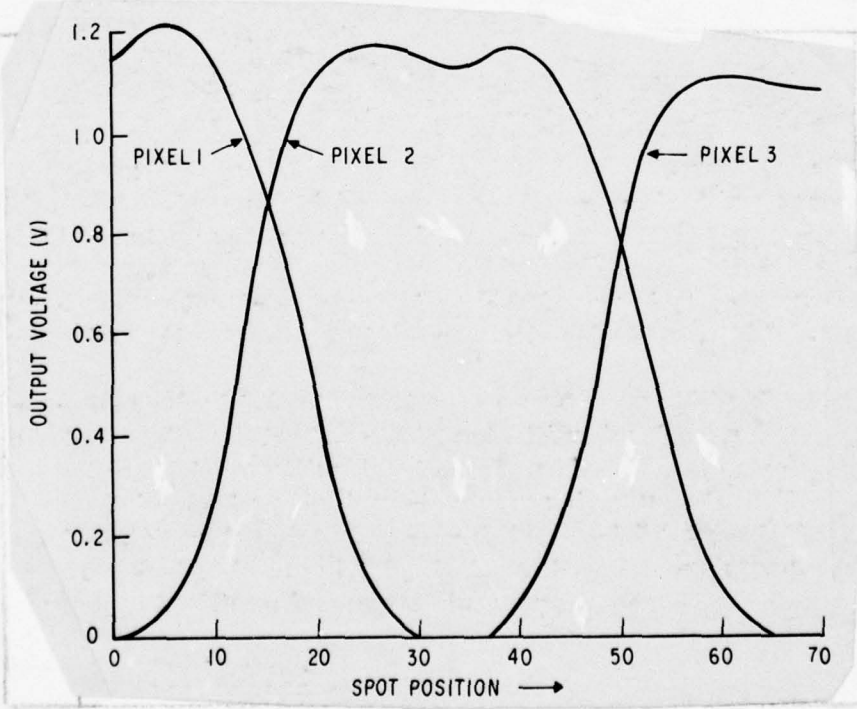


Figure 5-4. Point Spread Function, Vertical

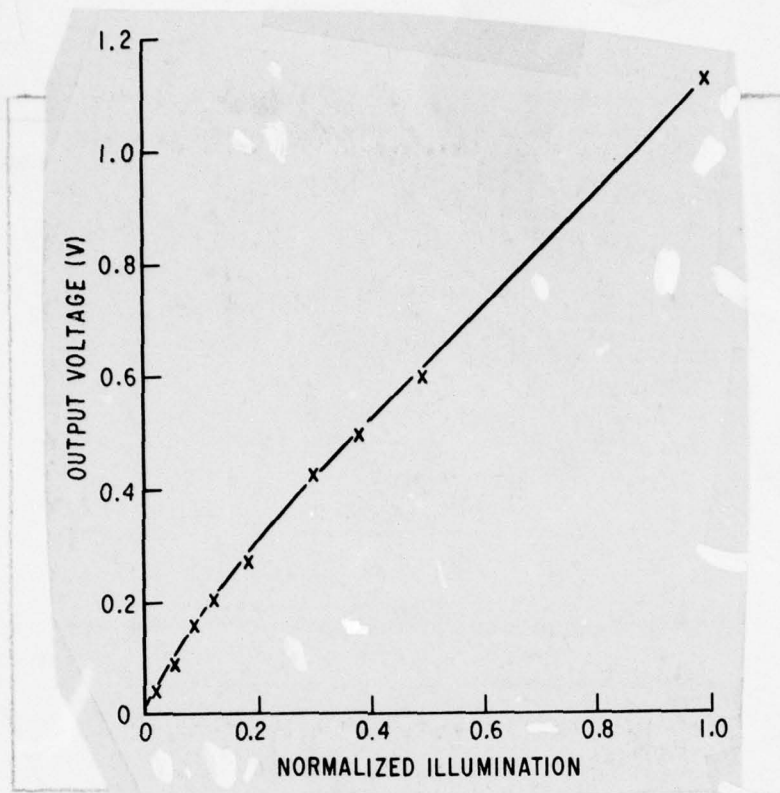


Figure 5-5. Transfer Characteristics

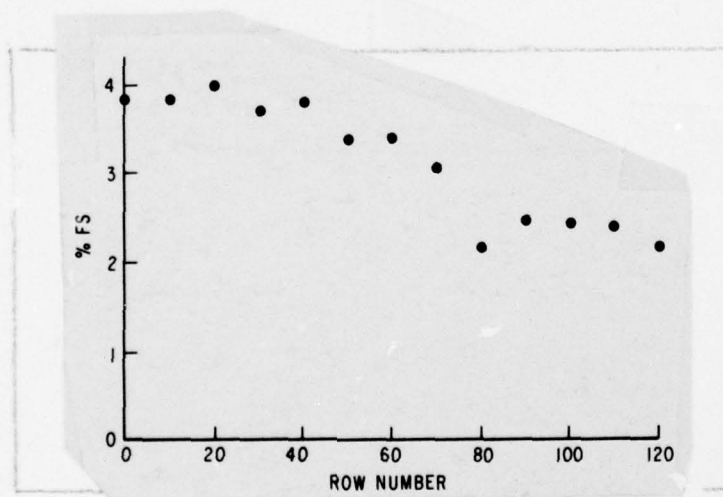


Figure 5-6. Element-to-Element Variations in Fixed Pattern Noise

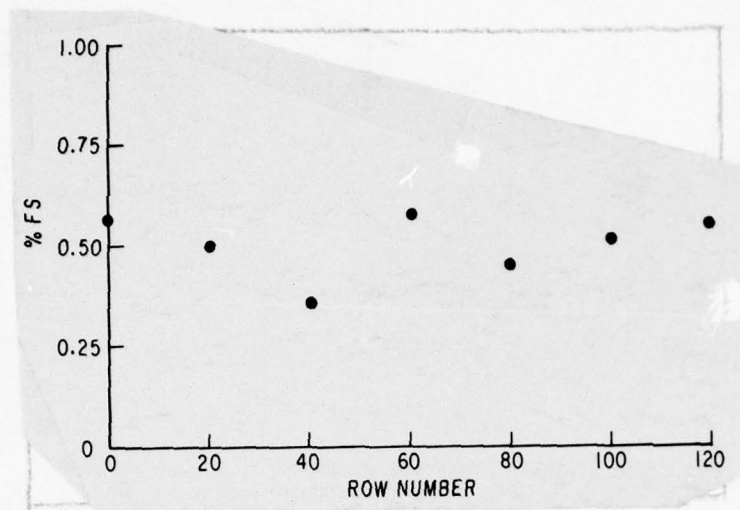


Figure 5-7. Element-to-Element Variations in Sensitivity



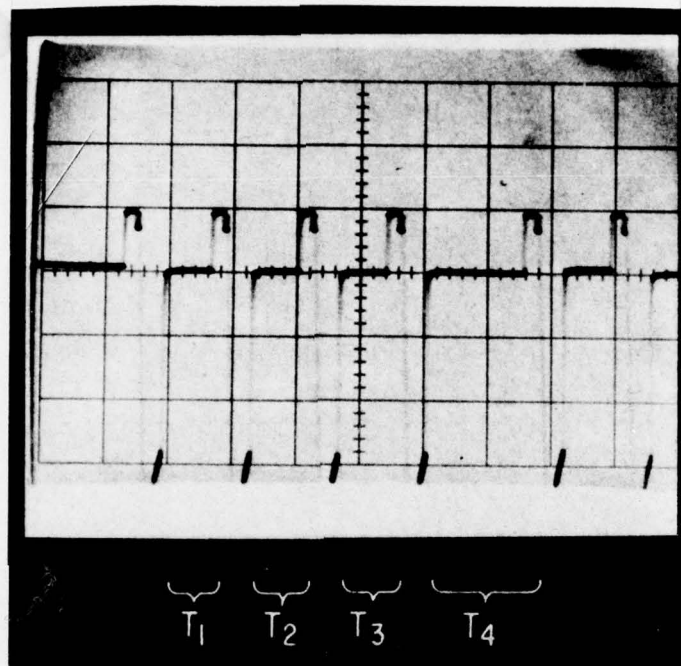
Figure 5-8. Typical Image, Normal Readout

due to localized dark current can be seen. Unfortunately, the wide dynamic range and low dark current measured on the video signal cannot be shown due to limitations of the image reproduction system used.

5.2 IMAGER PERFORMANCE - TRANSFORM READOUT

Several devices from lot 3 were tested in the transform camera. All imagers tested demonstrated that the spatial transform was being taken. Each Hadamard transform value is simply a binary summation of the analog signals from a group of pixels. Thus, the weighting factor of each analog signal is +1 or -1. A one-dimensional transform of a four element block is accomplished as follows. The first transform point (T_1), the lowest spatial frequency or DC level is the sum of the charge in each of the four elements

PC (++++). The next highest frequency (T_2) is the sum of the charge in the first two elements minus the sum of the charge in the second two elements (++--). The third transform point (T_3) is (+--+), and the fourth transform point (T_4), the highest spatial frequency, is (+--+). These results are summarized in Figure 5-9.



$$T_1 = P_1 + P_2 + P_3 + P_4$$

$$T_2 = P_1 + P_2 - P_3 - P_4$$

$$T_3 = P_1 - P_2 - P_3 + P_4$$

$$T_4 = P_1 - P_2 + P_3 - P_4$$

Where $T \equiv$ Transform Value

$P \equiv$ Pixel Value

Figure 5-9. Transform Readout Waveforms
(No Illumination)

In the present array structure, four of these one-dimensional transforms are read out in parallel, and a two-dimensional transform may be performed off-chip.

One way to verify transform operation is to illuminate only one of the elements in the four element block, and observe the four transform points on an oscilloscope. When the array is dark all four transform points are zero (see Figure 5-9). (The hold time for the fourth transform point is

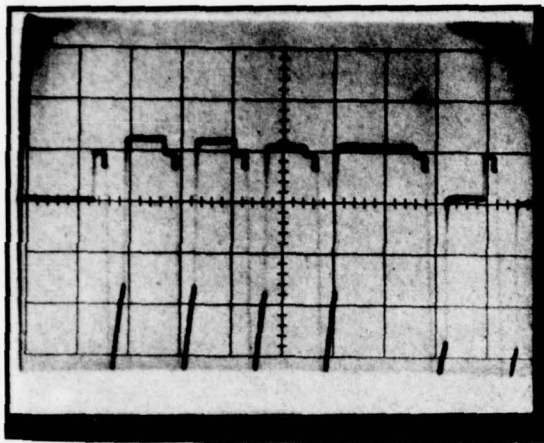
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longer than the hold time for the other three because the shift register must shift to the next four-element block during this time). When only the first of the four elements is illuminated, the first transform point, the sum of the charge in all four elements, will read +1 unit, on a normalized scale. The second transform point also will equal +1 unit, since the sum of charge in the first two elements is 1 and the sum of charge in the last two elements is 0. Similarly, the third and fourth transform points will equal +1 unit. This is shown in Figure 5-10(a). Now the light spot is moved so as to illuminate only the second element of the four. The first transform point is still +1 since the sum of the charge for the four elements is still +1 unit. The second transform point is also +1 unit. The third transform point is now -1 unit because it is the sum of the charge in the first and fourth element (0) minus the charge in the second and third element (1). Similarly the fourth transform point is -1. This is shown in Figure 5-10(b). When the light spot illuminates the third element only, the transform points are +1, -1, -1, and +1 respectively [Figure 5-10(c)]. Finally, when the light spot illuminates only the fourth element the four transform points are +1, -1, +1, and -1, respectively [Figure 5-10(d)]. It should be emphasized that the waveforms of Figure 5-10 are sampled analog quantities. The very narrow point spread function of these imagers and the good transform readout quality results in uniform analog samples that should not be mistaken for digital signals.

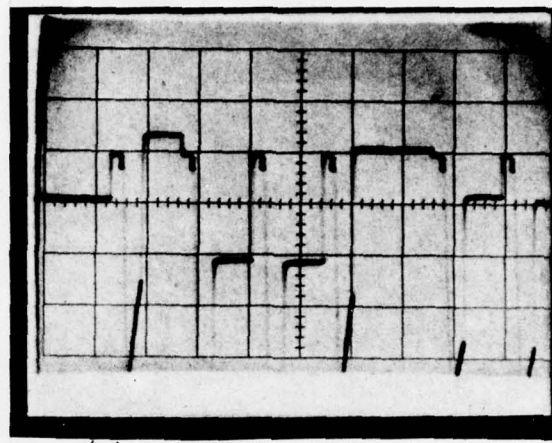
The performance characteristics of the imagers in the transform mode were measured when applicable. NDRO operation is inherent in the transform mode since each pixel must be read out repeatedly to produce the transform. Dark current levels and sensitivity are the same as for the normal mode.

Dynamic range measurements in the transform mode were hampered by a problem with the horizontal scanners. In this mode, where four columns must be driven simultaneously, parasitic coupling to the scanner outputs caused it to malfunction. Proper operation could be achieved by reducing the drive voltages, but this resulted in a lower dynamic range. Although performance was expected to improve due to the factor of 5 reduction in bandwidth, the limited drive capabilities offset this advantage and the dynamic range measurements were on the same order as those obtained in the normal mode.

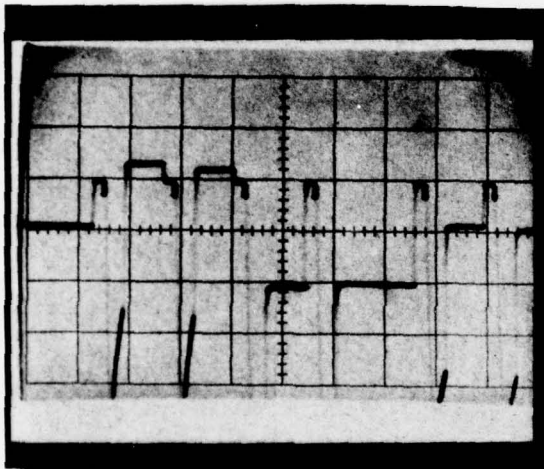
This scanner inadequacy can be corrected by a circuit modification in future designs.



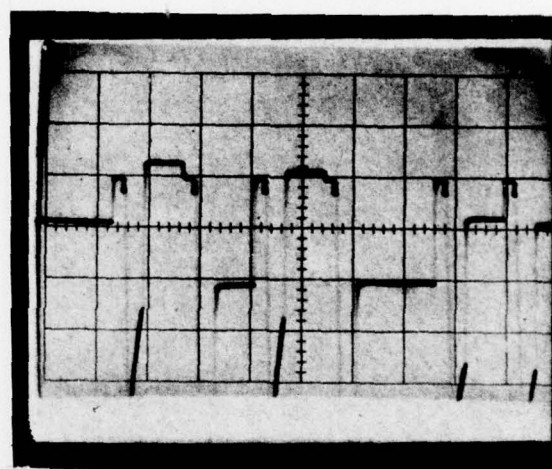
(a) First Pixel Illuminated



(c) Third Pixel Illuminated



(b) Second Pixel Illuminated



(d) Fourth Pixel Illuminated

Figure 5-10. Transform Readout Verification

Midon
SP0069

6.0 SUMMARY AND CONCLUSIONS

The feasibility of real-time transform coding of an optical image directly on a CID imager has been conclusively demonstrated. In addition, picture quality, in terms of thermal and fixed-pattern noise, MTF, and spectral response characteristics, is excellent. Two minor design deficiencies, not uncommon in new imager designs, were but a minor hindrance in characterizing device performance. These errors will be corrected in future designs.

The falloff in response at the shorter wavelengths, while expected from the two-level polysilicon structure, is nevertheless disappointing. Fortunately, the advent of transparent, metal-oxide electrode materials promises a dramatic improvement in the blue-green response of future devices.

Resolution of the present device is unlikely to be sufficient for a large number of potential applications; however, the design, with its $30\text{ }\mu\text{-square}$ sensing site size, can be relatively easily expanded to higher resolution -- to 256×256 and higher.

This development is considered to be an important first step towards the realization of miniature, low power, bandwidth-compression, (jam-resistant) systems suitable for mini-RPV applications. Other potential applications are in video-guided weapons and cannon-launched guided projectiles (smart bombs).

A scientific imaging application might be in Hadamard-transform spectroscopy, where the elimination of cumbersome optical masks would result in significant system simplifications.

Two areas in which future development is required are:

- (a) increased resolution through the design, fabrication, and evaluation of arrays of the order 256×256 .
- (b) evaluation of total systems performance of a bandwidth-compression system incorporating such a CID array, including assembly of a demonstration system.

APPENDIX A

1. SCANNER DESCRIPTION

As described in the text, selection of individual subgroups is effected by means of two serial shift registers fabricated along one horizontal and one vertical axis of the array. This particular design was developed for use on high-speed, high-density CID arrays and for this reason has some unique characteristics not found in the more normal type of MOS shift register.

An important observation can be made on the nature of the shift registers required in this application. As every line (row or column) must be addressed just once between consecutive initializations of the shift registers, it follows that a signal "one" is always trailed by a series of logic "zero" levels; more appropriately, therefore, we should call this circuit element a scanner instead of a shift register.

For this reason we can simplify the design of the scanner as we can impose without penalty on performance that each stage of the scanner following a logic level "one" be set at a logic level "zero." Furthermore, by designing this scanner with noninverting stages, the number of parallel outputs doubles in comparison to a similar register made with inverting stages. This is due to the fact that an output can be tapped only once for every pair of inverters, because the signal and its complement must be held at every stage.

A main concern in the design of a scanner is the regeneration of the signal at every stage for avoiding signal losses in the transfers, particularly those due to gate threshold drops. This problem is overcome with the introduction of bootstrapping in the form of a MOS varactor capacitor, which has the desirable property of being active only in presence of a signal "one." Thus a noise rejection mechanism is inserted in this scanner as the signal is transmitted and amplified only if it is above the gate threshold value.

This scanner is clocked by two phase lines with the clock pulses alternately fed to one or the other of the two lines. At any time there is always a phase line at ground level, making a separate ground bus line unnecessary.

The scanner circuit diagram is shown in Figure A-1. Four MOS transistors are the active elements of each stage. Two of them, called T_1 and T_3 , have large aspect ratios, because their purpose is to transfer the phase line clock pulse with the smallest delay to the next stage when the preceding stage is at logic level "one." Specifically, the gate of T_1 is connected to the gate of the bootstrapped MOS varactor T_4 , which can thus rise above the phase line voltage and transfer without threshold losses and at high speed the clock pulse through T_1 . For achieving a significant bootstrapping action

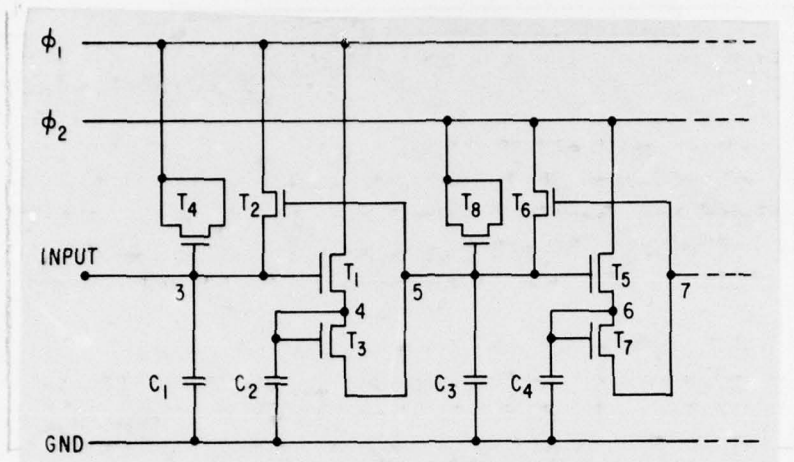


Figure A-1. Scanner Circuit Diagram

the combined gate capacitance of T_4 and T_1 should be large in comparison to the other capacitances associated with the same node, but coupled to the substrate (ground), like C_1 and C_{g2} . As the design of T_1 is largely dictated by the selection of an appropriate transconductance value, the main bootstrapping capacitance is provided by T_4 which is laid out as a large area device with aspect ratio close to one and with source and drain tied together. As T_4 acts like a charge reservoir, the square geometry provides an optimum charge access to the output port allowing shorter time delays in charging and discharging.

Transistor T_3 is connected in a diode configuration with the gate and the drain tied together. As a result it allows the charging of node 5 to take place, but it cuts off the discharge path, electrically isolating this node during the falloff of the phase pulse ϕ_1 .

Finally, transistor T_2 provides a discharge path for the bootstrapping capacitance bringing the gate voltage of T_4 and T_1 to ground after the charging of node 5 has taken place. This transistor should be designed with minimum geometry, because it is turned on after node 5 has been electrically isolated during the falloff of the phase pulse ϕ_1 and therefore reduces the bootstrapping action of T_8 by coupling node 5 to the ground.

The aspect ratio of transistor T_2 should also be small in comparison to that of T_1 for assuring that T_1 completes the discharge of node 4 before it is turned off by the simultaneous discharge of node 3 through T_2 . In practice, T_2 is designed with an aspect ratio of 1, while T_1 and T_3 have approximately an aspect ratio of 6 to establish a safe margin in the time constants ratio.

As we refer to p-channel devices, let us consider that in the initial condition the input voltage V_3 is negative and equal to V_O which is equivalent to a logic level "one." As a result transistor T_4 is "on" determining a strong

Michon/BB (A-3)

capacitive coupling between the input phase line ϕ_1 . This coupling is due to the formation of an inversion layer beneath the gate of T_4 , which can be interpreted as an extension of the source and drain regions in the computation of the gate-source (drain) capacitance.

As the phase line ϕ_1 is pulsed from 0 to V_{ϕ} , the large capacitance of T_4 overrides the capacitance to ground C_1 and bootstraps V_3 to V_{BS} which must be larger than V_{ϕ} for a complete transmission of pulse ϕ_1 through transistor T_1 without threshold losses. The harder T_1 is turned "on," the shorter is the lag in the rise time of pulse ϕ_1 at node 4. Transistor T_3 is connected in a diode equivalent configuration between nodes 4 and 5 and is "on" when V_4 is more negative than V_5 by at least a threshold voltage, V_T .

Thus under the influence of pulse ϕ_1 transistor T_3 conducts and draws current from node 4 for charging C_3 and the gate to source (drain) capacitances of T_5 and T_8 . It will eventually stop conduction when V_5 equals $(V_{\phi} - V_T)$, assuming that the gate of T_3 is at V_{ϕ} .

Transistor T_2 is turned off during the ϕ_1 pulse, because even when the gate is at the peak voltage $(V_{\phi} - V_T)$, this voltage is still less than the source and drain voltages, V_{ϕ} and V_{BS} respectively. Thus any current drain is precluded from node 3, and the bootstrap voltage remains constantly applied to the gate of T_1 until the pulse ends.

When the phase line ϕ_1 falls back to zero, transistor T_3 is turned off immediately, letting the voltage at node 5 to reach its equilibrium value V_O as a result of charge redistribution between C_3 and the capacitances of transistors T_2 , T_5 , T_8 , and in smaller degree, of T_3 . Simultaneously, V_3 is brought back to its initial voltage, V_O , as the bootstrapping action of T_4 now occurs in reverse, and from this level V_3 falls rapidly to zero as the charge at node 3 drains through T_2 , which is now "on."

The voltage at node 4, V_4 , is also decreasing rapidly to zero as C_2 and the capacitance of T_3 are discharged through transistor T_1 to phase ϕ_1 , which is now zero. Caution must be exercised in the scanner design to ensure that V_3 does not fall to zero faster than V_4 , because as soon as V_3 is within a threshold drop from ϕ_1 , T_1 is turned "off" freezing the residual voltage V_4 . This problem is avoided by choosing a much larger aspect ratio for T_1 than for T_2 and by keeping C_2 reasonably small.

When the phase pulse ϕ_2 starts, the bootstrapping action raises V_5 from V_O to V_{BS} , repeating the cycle already described for V_3 and pulse ϕ_1 .

For completeness, let us consider the case where in the initial condition V_3 is below threshold, corresponding to a logic level "zero." As transistor T_4 is then turned "off," the bootstrapping action does not occur in presence of pulse ϕ_1 and coupling between node 3 and ground through C_1 prevails in

keeping V_3 below threshold so that transistor T_1 remains "off" and no voltage change occurs in the following stages of the scanner.

Examining the timing diagram, Figure A-2, we observe the existence of two types of pulses, which can be used as outputs on a capacitive load -- for example, the gate of a decoder transistor. This feature adds considerable flexibility to this scanner, because in some applications it is preferable to have output pulses at adjacent locations which are slightly overlapping in time, like V_3 , V_5 , and V_7 , while in other cases a complete extension of a pulse is required before the next pulse starts at the following output, like V_4 and V_6 .

This design has been thoroughly evaluated, both analytically and by means of various computer-aided transient analysis programs, (such as SCEPTRE), and is used in a number of operational CID imagers. The particular design used in the subject array was fully evaluated and its performance verified for the application.

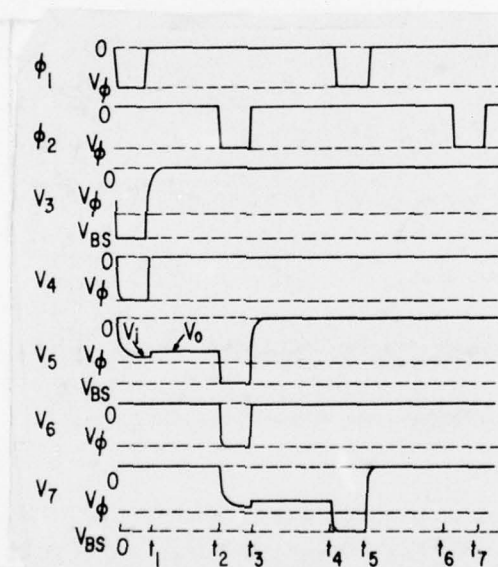


Figure A-2. Scanner Timing Diagram

Michon/68 (B-1)

APPENDIX B

ARRAY OUTPUT CAPACITANCE

The capacitive load presented to the signal charge and any on-chip voltage attenuation must be known to determine array performance factors such as quantum efficiency, dark current density and noise equivalent signal. The array schematic diagram, Figure B-1, illustrates the on-chip circuitry used to connect four array rows to the on-chip MOS-FET source followers. A single logical "ONE" is transferred along the vertical scanner to sequentially select the array rows in groups of four. The selected group of four rows is connected to four source follower MOS-FET gates providing that the disconnect gate (DG) is energized. The injection gate (IG) is off during array readout. A compensation line (C) has been added to the array to provide for cancellation of the capacitively coupled column drive voltage interference. This compensation line is selected by a logical "OR" of the vertical phase drive voltages so that it is active for all array readout operations. The compensation signal bus line was located inboard of the row signal bus lines to insure that the compensation bus would have a distributed capacitance that was similar to the active row signal bus capacitance. The cross-coupling between the signal lines and the compensation line that was introduced by this choice of compensation bus location resulted in signal attenuation prior to on-chip amplification. It resulted in a significant loss in dynamic range, approximately 2:1, and a small amount of crosstalk between the four array rows being read out. These problems can be effectively eliminated in future array designs by a simple topological layout change. The magnitude of the on-chip capacitance and voltage attenuation was measured to allow characterization of chip parameters.

The equivalent circuit of the row selection network is shown in Figure B-2. One packaged imager was biased in the normal manner and the magnitude of the capacitance components was determined as follows:

1. The capacitance of all array rows was measured at terminal RVD. The individual row capacitance, C_R , was found to be $C_R = C_{RVD}/128 = 6.0 \text{ pF}$.
2. The sum of the four signal and compensation bus line capacitance, including the gate input capacitance of the on-chip source followers was measured at terminal ID.

$$C_C + 4C_S = 21.8 \text{ pF}$$

3. The capacitance, looking into the compensation line, was measured through terminal C.

$$C_{\text{measured}} = C_C + 4 \left[\frac{C_X C_S}{C_X + C_S} \right] = 7.3 \text{ pF}$$

4. The ratio of crossover capacitance, C_X , to signal bus capacitance, C_S , was measured by capacitively coupling a small voltage pulse into

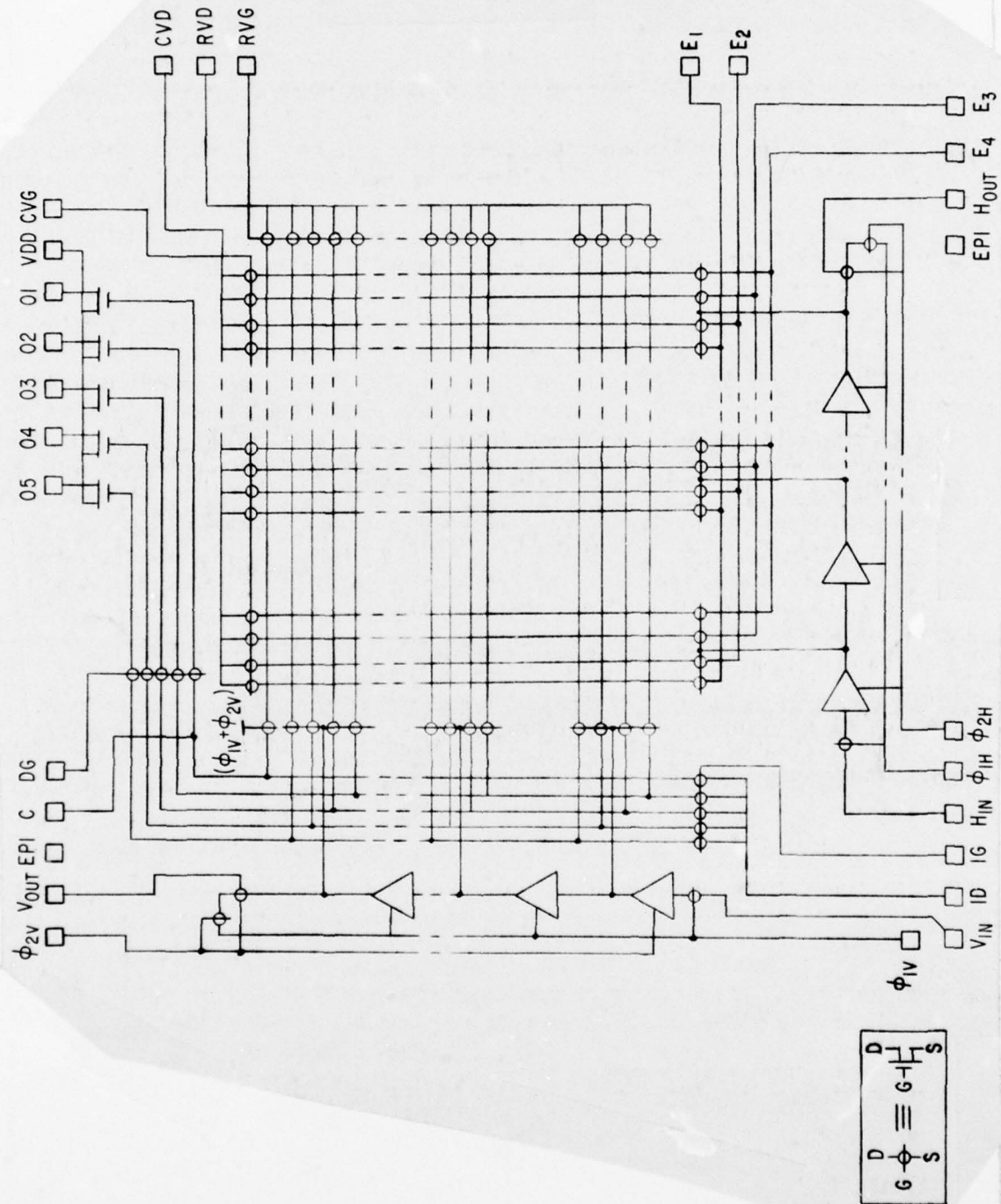
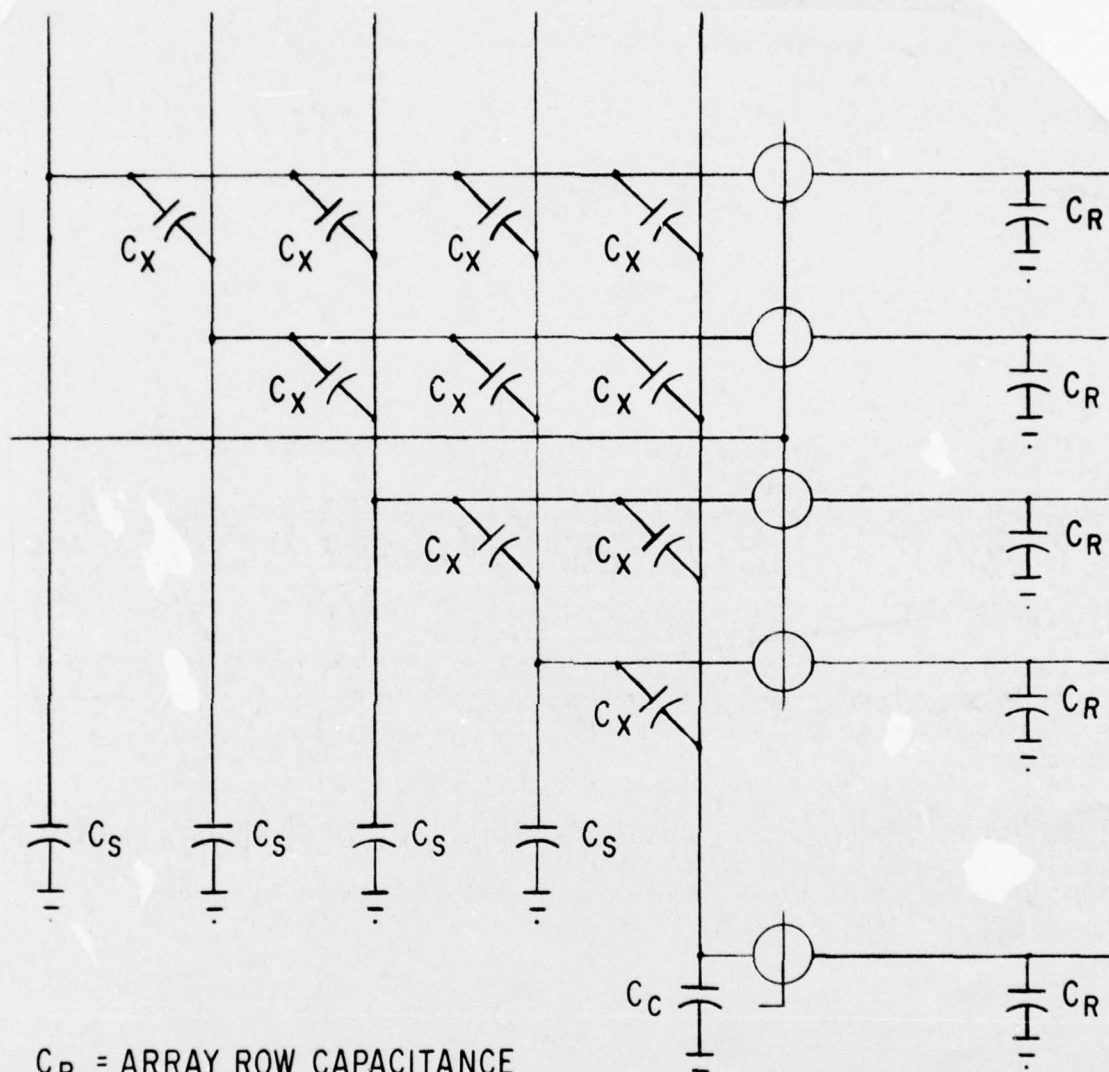


Figure B-1. Array Schematic Diagram



C_R = ARRAY ROW CAPACITANCE
 C_S = SIGNAL BUS LINE CAPACITANCE
 C_C = COMPENSATION BUS LINE CAPACITANCE
 C_X = CROSS-OVER CAPACITANCE

Figure B-2. Row Selection Network Equivalent Circuit

terminal C and measuring the ratio of source follower output 01 to outputs 02 through 05. The circuit was maintained at normal bias voltage during this measurement by periodically pulsing IG while maintaining ID at the row bias voltage. The measured ratio of output 01 to 02 through 05 was 3 to 0.8 for all four signal outputs.

Michael/B3 (B-4)

$$3 \left[\frac{C_x}{C_s + C_x} \right] = 0.8 ; \frac{C_x}{C_s} = \frac{4}{11}$$

From this data the array capacitive components was found to be

$$C_R = 6.0 \text{ pF}$$

$$C_s = 4.9 \text{ pF}$$

$$C_c = 2.0 \text{ pF}$$

$$C_x = 1.8 \text{ pF}$$

A source follower voltage gain of 0.82 was also measured under these conditions.

When an area of the array is illuminated uniformly, all four signal bus lines will have the same video voltage and the cross-coupling capacitance between signal lines will not act as load capacitance. Signal voltage is coupled from all four signal bus lines to the compensation line resulting in a fraction of the signal voltage appearing on the compensation line. Under this condition, the compensation line voltage is:

$$V_c = V_s \left[\frac{4C_x}{C_R + C_o + 4C_x} \right] = .48 V_s$$

Since the compensation line voltage is subtracted from the four signal line outputs, the effect of this cross-coupling is to attenuate the signal by approximately two to one. The total on-chip gain, including the source follower, is

$$\begin{aligned} & \left(\frac{V_s - V_c}{V_s} \right) \times \text{Source follower gain} \\ & = \left(\frac{V_s - .48 V_s}{V_s} \right) \times .82 = .43 \end{aligned}$$

The loading effect on the cross-coupling capacitance from one signal line to the compensation line is:

$$C_x \left(1 - \frac{V_c}{V_s} \right) = 0.9 \text{ pF}$$

The total load capacitance under uniform illumination conditions is:

$$\begin{aligned} C_{\text{LOAD}} &= C_R + C_s + C_x \left(1 - \frac{V_c}{V_s} \right) \\ &= 11.9 \text{ pF} \end{aligned}$$

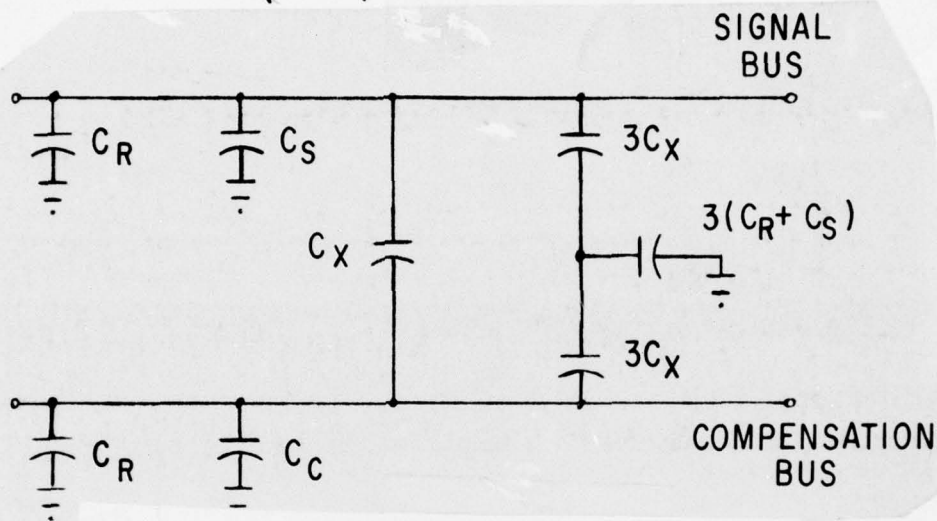
Under point source illumination conditions the cross-coupling capacitance between signal bus lines does load the signal charge. The equivalent circuit for one signal bus is shown in Figure B-3(a). This equivalent circuit has been simplified by applying a Y - Δ transformation. The result is shown in

Figure B-3(b). Substitution of the measured capacitance values results in the following load capacitance and gain factors.

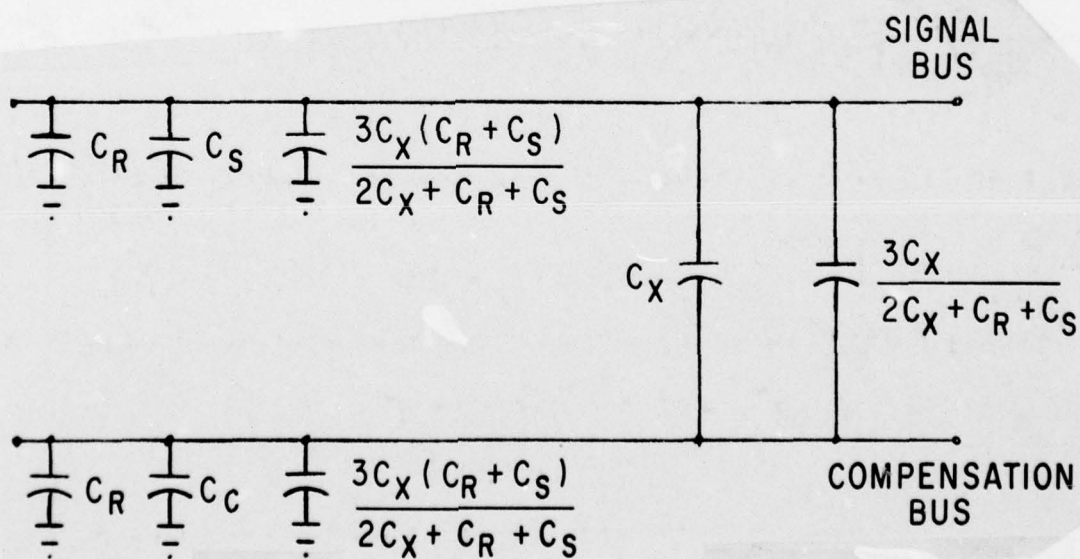
Signal Load Capacitance, $C_S = 17.1 \text{ pF}$

Signal on Compensation Line, $V_C = .17 \text{ V}_S$

$$\text{GAIN} = \left(\frac{V_S - V_C}{V_S} \right) \times \text{Source Follower Gain} = .68$$



(a) Capacitive Loading & Cross-Coupling



(b) Simplified Circuit

Figure B-3. On Chip Equivalent Circuit - Point Illumination